System and Circuit Approaches for the Design of Multi-mode Sigma-Delta Modulators with Application for Multi-standard Wireless Receivers

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Abstract

This thesis is mainly concerned with discrete time sigma-delta modulators aimed for the digitisation of narrow- and wide- band signals present in multi standard wireless receivers. For this purpose, a receiver architecture is proposed, where the analogue to digital conversion of narrow band signals is carried out at low values of intermediate frequency, while wide-band signals are being converted at zero-IF.

In order to preserve the low power consumption requirements demanded by mobile terminals, an A/D converter able to reach high values of signal-to-noise ratio by using modest oversampling ratios is needed. Another characteristic, that should be exhibited by the converter is flexibility, since it has to work in a multi mode environment handling with different intermediate frequencies, channel bandwidths and modulation techniques.

Single Bit High Order sigma-delta Loops appear to be good candidates to full fill the mentioned needs. They are able to achieve high values of *SNR* for low *OSR*s and their circuit implementation is very robust. They also have the interesting characteristic of synthesizing different types of noise transfer functions by changing the filter loop coefficients without altering the structure of the modulator.

In order to improve both resolution and stability of single bit high order $\Sigma\Delta$Ms, quantization noise suppression should be carried out not only at DC but also within the band of interest. This noise suppression at frequencies different form zero is carried out with the use of *resonators*. Switched Capacitor resonators at f_s/n can be designed using integrating or delaying elements.

In this work, both resonator structures were analysed with respect to their robustness against the main imperfections presented in a SC implementation. The effect introduced by the operational transconductance amplifiers (OTAs) nonidealities was analysed together with the effect of capacitor mismatch.

Due to their importance in the design of bandpass sigma-delta modulators, there has been a great interest in analysing the different existing structures to synthesize resonators at frequencies around $f_s/4$, but this is not the case for resonators at frequencies different from one quarter of f_s. However, resonators at f_s/n are important for the digitisation of wide band signals in current

and future wireless communications systems because its conversion is more easy to accomplish at base band or low IF than at high IF values situated around $f_s/4$.

The conducted study shows the superior performance of the integrator based resonator over delay based structures. The robustness exhibited by this resonator at frequencies within baseband makes it a good candidate for the implementation of wide band ADCs whose OTAs encompass moderate voltage gain and a unity gain frequency around four times f_s. Such values are not very difficult to reach in current sub micrometric technologies using well known single stage OTA topologies.

Using the integrator based resonator and the ability of single bit loops to synthesize different NTFs by changing the coefficient set, a prototype of a 4^{th} order multi-mode $\Sigma\Delta$ modulator was designed. Care was put in this design in producing a flexible prototype, which could be used for the conversion of both narrow and wide band signals with reasonable power consumption using simple circuit structures. This experimental prototype was fabricated in a 0.35μm CMOS technology using a core area of 0.19sqmm. It consumes 48.6mW from a single 3.3V power supply and achieves a peak *SNR* of 72dB over a bandwidth of 200 kHz when clocked at 16 MHz. For wideband signals the measurements showed a resolution of 53dB if the bandwidth extends to 1.92 MHz, as required by UMTS signals. In this case the prototype was clocked at 76.8 MHz, which produces an *OSR* of 20.

Kurzfassung

Die vorliegende Arbeit befasst sich mit Analyse, Modellierung und Entwurfsmethodik von Sigma-Delta-Modulatoren für die analog-digital Umsetzung von schmal- und breitbandigen Signalen in der Mobilfunktechnik.

Es wird eine Methode vorgeschlagen, welche die A/D Wandlung schmalbandiger Signale zentriert um niedrige Zwischenfrequenzwerte durchführt. Die Umsetzung breitbandiger Signale wird mit einer Zwischenfrequenz von null realisiert.

Die Anforderungen an die A/D Wandler heutiger Mobilfunksysteme sind eine hohe Auflösung, niedriger Leistungsverbrauch und Flexibilität. Einzel-Bit Sigma-Delta-Modulatoren hoher Ordnung profilieren sich als gute Kandidaten um diese Anforderungen zu erfüllen. Sie können hohe Auflösung mit einer niedrigen Überabtastrate erreichen, ihre schaltungstechnische Realisierung ist sehr robust und sie können für verschiedene Rausch- Übertragungsfunktionen durch einfaches Ändern des Koeffizientensatzes verwendet werden.

Zur effizienten Unterdrückung des Quantisierungsrauschens benötigen einzel-Bit Sigma-Delta Modulatoren hoher Ordnung aktive Resonatoren im Basisband. Diese Resonatoren werden in der Regel als Integratoren oder als Abtast- und Halteschaltungen in Switched-Capacitor-Technik realisiert. In der vorliegenden Dissertation werden diese resonanten Strukturen in Bezug auf Robustheit gegen nicht-ideale Effekte der schaltungstechnischen Realisierung analysiert.

Zum Vergleich wurden beide Konzepte in einem Sigma-Delta-Modulator vierter Ordnung in Switched-Capacitor-Technik simuliert. Die durchgeführte Untersuchung zeigt die bessere Leistung der auf Integratoren basierten Resonatoren im Basisband. Der daraus entworfene Schaltkreis ist geeignet für die A/D Umsetzung von Basisbandsignalen nach GSM, Bluetooth und UMTS Standard und wurde in einer 0,35μm CMOS Technologie als Test-ASIC gefertigt.

Das gefertigte Muster verbraucht 48,6mW Leistung und benötigt eine einzige 3,3V Spannungsversorgung. Die gemessene (nutzbare) Auflösung ist 53 dB für eine Taktfrequenz von 78.6 MHz innerhalb einer Bandbreites von bis zu 1.92 MHz.

Acknowledgement

The present thesis was developed during my stay as research assistant at the Institute of Microelectronic Systems (MES) of the Darmstadt University of Technology, under the supervision of Prof. Dr. Dr. h.c. mult. Manfred Glesner, whom I would like to thank for the overall advisement of this work and for the financial support given during the last 18 months of my research at his institute.

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Finally I want to express my gratitude to my family, relatives and friends in Mexico. They were always with me during my absence these years. My friends in Germany played also a very important role all these years, thank you.

Nomenclature

AAF	Anti Alias Filter
AC	Alternate current
ADC	Analog to digital converter
ADSL	Asymmetric Digital Subscriber Line
AGC	Automatic Gain Control
AM	Amplitude Modulation
BB	Base band
BPΣΔ	Bandpass Sigma-Delta
BPΣΔM	Bandpass Sigma-Delta Modulator
BT	Short range ubiquitous connectivity standard, Bluetooth
CMOS	Complementary Metal-Oxide-Semiconductor
CT	Continuous time
DAC	Digital to analog converter
DSMP	Dual standard mobile phone
DSP	Digital signal processing
FM	Frequency Modulation
GSM	Global System for Mobile Communications
IF	Intermediate Frequency
LDI	Lossless discrete integrator
LNA	Low Noise Amplifier
NF	Noise Figure
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PPF	Passive polyphase filter
PSRR	Power supply rejection ratio

RF	Radio Frequency
SAW	Surface Acoustic Wave
SC	Switched Capacitor
SFDR	Spurious-Free dynamic range
SH	Superheterodyne
SSH	Single IF superheterodyne
SwR	Software Radio
UMTS	Universal Mobile Telecommunications System
VLSI	Very large scale of integration
WCDMA	Wide-band Code Division Multiple Access Technology
A_V	Voltage Gain
BW	Bandwidth
C_{in}	Input capacitance
$CPI_{(a)}$	The Chip performance index (analog)
$CPI_{(RF)}$	The Chip performance index (RF)
DR	Dynamic Range
$ENOB$	Effective number of bits
FFT	Fast Fourier Transform
FoM	Figure of merit
I	In-phase component of a complex signal
$IP3$	Third order intercept point
N_e	Quantization noise power spectral density
NTF	Noise Transfer Function
OSR	Oversampling Ratio
P	Power consumption
P_e	In-band quantization noise power
PM	Phase margin
Q	Quadrature-phase component of a complex signal. Quality factor
$SNDR$	Signal to noise and distortion ratio
SNR	Signal to noise ratio
$SQNR$	Signal to quantization noise ratio
SR	Slew rate
STF	Signal transfer function
T	Absolute temperature
V_{dd}	Power supply voltage
Vds_{sat}	Saturation voltage
V_q	Quantization voltage
V_{REF}	Full scale input/output range of a quantizer

V_T	Threshold Voltage
f_b	Baseband cutoff frequency
f_s	Sampling frecuency
f_u	Unity-gain frequency
g_m	Small signal transconductance
g_mC	Transconductor capacitor
i_b	Bias current
k	Boltzmann's constant
r_O	Small signal output resistance
$1/f$ noise	Flicker Noise
2G	The second generation of mobile communications systems
3G	The third generation of mobile communications systems
Δ	Quantization step size
$\Sigma\Delta$	Sigma-Delta
$\Sigma\Delta$M	Sigma-Delta Modulator
β	Feedback factor
δ	Gain error produced by finite A_V in a delay cell
ε	Gain error produced by finite f_u in an integrator
ε_d	Pole error produced by finite A_V in an integrator
ε_n	Gain error produced by finite A_V in an integrator
γ	Gain error produced by finite f_u in a delay cell
μ	Micro (10^{-6})
σ_e^2	Quantization noise power

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Contents

1.1 Motivation

During the last two decades, the rapid evolution of digital integrated circuit technologies has led to ever more sophisticated signal processing systems. These systems operate on a wide variety of continuous time signals including voice, medical imaging, sonar, radar, electronic warfare, instrumentation, consumer electronics and both terrestial and satellite telecommunications. This last area has drawn the most significant benefit and currently a wireless communication "explosion" is being experienced, where new services are being constantly introduced thanks to the availability of new integrated circuits and systems. A key component for the success of these systems has been the analog to digital converter (ADC) that converts continuous time signals to a discrete time, binary coded form for later digital signal processing. The large number of signal types to be digitized has led to a diverse selection of data converters in terms of architectures, resolution and sampling rates. In the wireless communications arena transmitters and receivers in general, and ADC's in particular, have to cope with the requirements imposed by many different standards operating in the same geographical zone, making it necessary for mobile communications equipment to manage multiple standards. A solution to this problem is the usage of the software radio (SwR) concept [1], that is based in the early analog to digital conversion of the incoming signals and its later processing by highly reconfigurable digital systems (fig. 1.1).

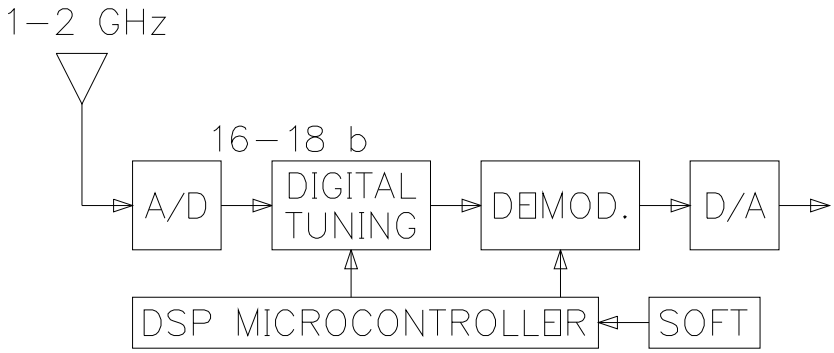

Figure 1.1: The software radio concept

The figure above presents the conversion of a radio frequency signal to the digital domain directly at the receiver antenna or after some amplification stages. After this conversion, all other operations needed to detect and recover the desired signal are performed in a fully digital fashion, by means of programmable hardware. This would allow the upgrading of a mobile terminal completely by software following the evolution of the communications standards, as well as its adaptability to different operating environments and avoiding so the obsolescence. Having in mind that signals at the antenna of a current mobile phone are situated on the order of several hundreds of megahertz or even up to some gigahertz, without forgetting the resolution imposed by the standards, which could be as high as 16 bits, then is impossible to imagine an ADC running at the radio frequency speed and delivering such a high resolution.

There have been many efforts to overcome the problem of digitising a radio frequency signal, at first glance, one could take a traditional radio reception approach and introduce the ADC at a point where the required speed and dynamic range were reachable with the current state of the technology. In fact, this has brought the development of different radio architectures, where the analog to digital conversion has been realized after some stages of analog signal processing already presented in the traditional radio receivers [2]. In this way, the translation of the signals to the digital domain has been accomplished at base band (BB) or intermediate frequency (IF), where the speed requirements are not so stringent. These architectures have been successfully applied to the single-standard mobile phones of the first and second generation. However, the introduction of analog hardware in those receivers represents a problem when trying to manage different standards, because it implies the replication of the involved hardware. Although the upcoming third generation (3G) of mobile communication services represents a great effort to introduce a unified standard, it is not expected that all suburban and rural areas are going to be covered by the new services of the (3G) and then, the second generation (2G) is also going to be present demanding for receivers capable of handling standards coming from both systems. This problem has already been addressed and the proposed solutions include the duplication of analog building blocks [3] with the required characteristics for each standard, as well as the use of analog circuitry capable to operate in both modes [4]. The analog to digital conversion stage

has been put also at different points of the receiver chain, namely at high [4] and low [5] IF values as well as at BB [3]. But the development of a fully integrated multi-mode radio receiver and the optimal position of the ADC, within a multi-mode receiver, to achieve the best trade off between speed of operation and resolution is still to be seen.

The new approaches developed to deal with this problem must be based on the experience collected by the already existing solutions and the path marked by the technology. The aggressive scaling, that the CMOS technology has seen in the last three decades, has a different impact over the performance of the components comprised by a radio receiver. In [6], Lu extended the *Chip Performance Index* (CPI) concept, originally proposed by Meindl for digital circuits, to analog and RF circuits in order to analyze its behaviour as technology is scaled. In that paper, the systems taken as case-study were pipelined ADC's as representive system for analog chips and LNA's and single-chip RF front ends for RF circuits. The *CPI* for analog circuits was defined as:

$$CPI_{(a)} = \frac{S/N}{P \cdot \tau} \qquad [\mathrm{J}^{-1}] \tag{1.1}$$

where S/N is the signal-to-noise ratio, P the reported power consumption and $\tau = 1/f_s$. Equation 1.1 was applied to published data from designs developed with different technologies. The obtained result revealed that, the $CPI_{(a)}$ generally improves as technology is scaled, but the $CPI_{(a)}$ of the best designs for each technology generation reaches a barrier regardless of device scaling (Fig. 1.2).

For radio-frequency chips, a simplified $CPI_{(RF)}$ was also developed to study the behavior of RF IC's:

$$CPI_{(RF)} = \frac{1}{P \cdot \tau \cdot (NF - 1)} \qquad [\mathrm{J}^{-1}] \tag{1.2}$$

Here, NF states for noise figure and $\tau = 1/f_{cen}$. Equation 1.2 was also used to evaluate the impact of scaling in designs carried out in different technological processes. Figure 1.3 shows the results of such evaluation, which tell us the following: while technology is improved, the noise-level-suppression capability per unit of energy consumption is improved in both CMOS LNA chips and single-chip receivers.

These valuable results should be taken under consideration by proposing new solutions to the already mentioned problem. They should also encourage the exploration of receiver architectures, in which, the benefits confered by scaling to the RF systems could be adequately exploided.

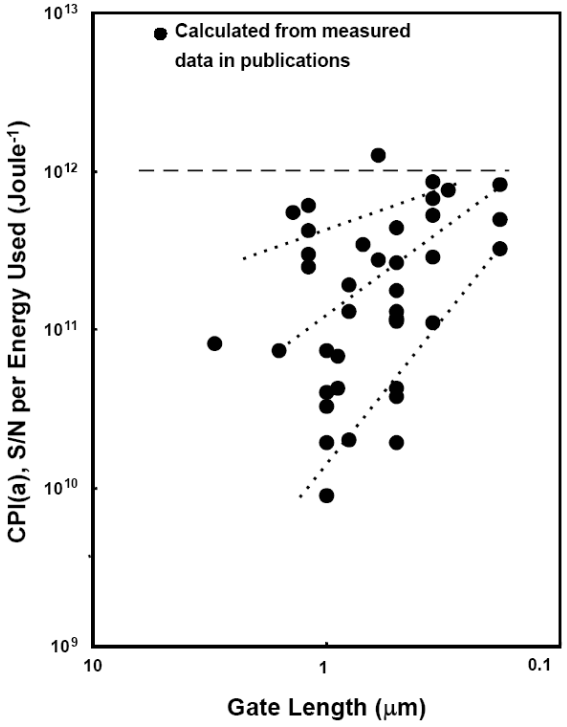

Figure 1.2: The chip performance index (analog). Reprinted from [6].

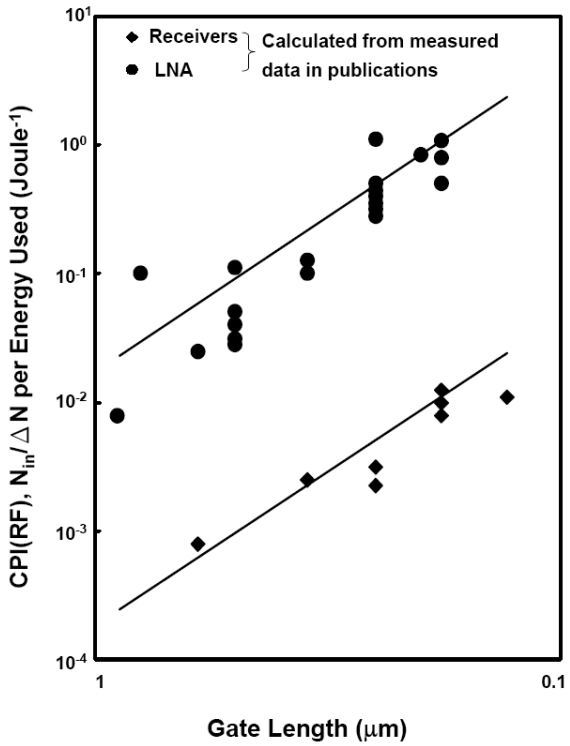

Figure 1.3: The chip performance index (RF). Reprinted from [6].

1.2 Research Goals

This work was mainly focused on the analysis, modelling and design of ADC's aimed for multi-mode wireless receivers. In the wireless communications area, analogue to digital conversion is being accomplished by means of oversampled sigma-delta ($\Sigma\Delta$) A/D converters.

Although the benefits of oversampling in A/D conversion are well known, the increasing bandwidth of the signals to be converted in the communications systems, as well as the required resolution imposed by the standards, ask for high oversampling ratios. Elevated sampling frequencies can compromise the low power consumption constraints of portable systems. One of the primary objectives of this work was to investigate the available architectures of $\Sigma\Delta$ converters, that enable to reach enough resolution with fairly low oversampling ratios, in order to preserve low power consumption.

Single Bit High Order $\Sigma\Delta$ Loops appeared to be very good candidates to full fill the mentioned requirement. They are able to reach high values of *SNR* for modest *OSR*s and their circuit implementation is very robust.

In order to improve both resolution and stability of single bit high order $\Sigma\Delta$M's, quantization noise suppression should be carried out not only at DC but also within the band of interest. This noise suppression at frequencies different form zero is carried out with the use of *resonators*. The literature reports mainly two structures for the design of switched capacitor resonators at f_s/n namely, The *Integrator Based Resonator* [7, 8] and *The Delay Based Resonator* [9, 10].

In this work, both resonator structures were analysed with respect to their robustness against the main imperfections presented in a SC implementation. The effect introduced by the finite voltage gain (A_V), non zero input capacitance (C_{in}) and finite unity gain frequency (f_u) of the operational transconductance amplifiers (OTAs) used in the implementation of those resonators, was analysed together with the effect of capacitor mismatch. It should be emphasized that, there has been a great interest in analysing the different existing structures to synthesize resonators at frequencies around $f_s/4$ because they are the fundamental elements needed in the design of bandpass $\Sigma\Delta$Ms [11], it is not the case for resonators at frequencies different from one quarter of f_s. However, resonators at f_s/n are important for the digitisation of wide band signals in current and future wireless communications systems because its conversion is more easy to accomplish at base band or low IF, than at high IF values situated around $f_s/4$. Traditionally, base band noise shapers have been designed using integrator based resonators. Applications of the delay based resonator at $f_s \neq f_s/4$ can be found in the literature [9],[10], but up to the point of writing this work, only the system level implementation was proposed, without any circuit implementation. Therefore, there was a lack of an analysis of the sensitivity of the delay based resonator to the imperfections of its SC implementation, when it produces frequencies different from that at $f_s/4$. A comparison with the classical integrator based construction used also at

f_s/n was also needed. These two points were fulfilled in this work. The conducted study shows the superior performance of the integrator based resonator over delay based structures. The robustness exhibited by this resonator at frequencies within baseband makes it a good candidate for the implementation of wide band ADC's whose OTA's encompass moderate A_V (60dB) and a value of f_u around four times f_s. Such values are not very difficult to reach in current sub micrometric technologies using well known single stage OTA topologies.

Another problem handled in this thesis was the flexibility required by the ADC's when used in mobile communications terminals. In this sense, single bit high order ΣΔM's become very attractive because they also have the interesting characteristic of synthesizing different types of NTF's by changing the filter coefficients without altering the structure of the modulator.

Using the integrator based resonator and the ability of single bit loops to synthesize different NTF's by changing the coefficient set, a prototype of a 4^{th} order multi-mode ΣΔ modulator was designed. Care was put in this design in producing a flexible prototype, which could be used for the conversion of both narrow and wide band signals with reasonable power consumption using simple circuit structures. This digitiser is aimed to operate in an original multi standard wireless receiver architecture [12], which was developed in a close related work [13], trying to follow the already mentioned tendencies announced by Lu.

In order to prove this ideas, an experimental prototype was fabricated in a 0.35μ double-poly triple-metal N-well CMOS technology. This design occupies an area of $1mm^2$ including bonding pads. Test and characterization of the proposed converter were also carried out. The obtained results show the feasibility of the proposed approach and open other fields for further investigations.

1.3 Organization

Given the motivation of this work and the research goals already mentioned, this thesis is organized as follows:

In order to review the main receiver architectures used in the mobile communications, as well as to have a general idea of how do they process the information signals, the following chapter brings an overview of the different methods used to detect and recover a radio-transmitted signal. Emphasis is done in the way those architectures manage the incoming signals after the antenna and the point at which the conversion of those signals to the digital domain takes place. As mentioned, by moving the ADC closer to the antenna, the presence of purely analog circuits is reduced, improving so the degree of integration and the flexibility exhibited by the receiver. However, the closer to the antenna the converter is located, the bigger are the requirements

of dynamic range and speed of operation imposed to the ADC, which in turn will define its required power consumption, an important constraint for portable systems.

As it will be pointed out in the chapter two, an omnipresent component of any modern radio receiver is the ADC. Analog to digital conversion of signals is not new and in fact, many methods exist to translate a real analog signal to a representation in a binary coded number. The nature of the application and the signal to be converted should always be a criterion to choose the most proper conversion method. As previously mentioned, due to their extremely high linearity and excellent spurious behavior, oversampled conversion methods combined with noise shaping, better known as sigma delta ($\Sigma\Delta$) converters, are the ones that dominate the wireless communications scenario. To understand the basics under these kind of converters as well as their properties, the chapter number three addresses the fundamentals of the analog to digital conversion with and without oversampling. Noise shaping techniques are also discussed to see why sigma-delta modulator ($\Sigma\Delta$M)-based ADC's are preferred over other techniques when applied to wireless systems. The experiment proposed by Galton [14] is reproduced, thus helping to clarify the excellent tonal behavior of $\Sigma\Delta$ ADC's reflected in a high spurious-free dynamic range (SFDR). Classical $\Sigma\Delta$M architectures are also analyzed and simulated showing the great linearity and dynamic range possessed by this kind of converters. As discussed in the chapter two, digitization of the information can be performed both in BB and IF, being for the last case, the so-called bandpass sigma-delta modulation (BP$\Sigma\Delta$), the most suitable conversion technique. This interesting case of the $\Sigma\Delta$ modulation is also presented and the classical architectures of such $\Sigma\Delta$M's are analysed and simulated as well.

As stated in section 1.1, the design of a radio architecture aimed for a multistandard receiver that fulfills the requirement of full silicon integration remains an open problem. The current efforts has been focused on designing architectures of dual standard mobile phones suited for the 2G and 3G of mobile communications services. Being this one of the main motivations of this work, the approaches reported in the literature, up to the point of writing this thesis, are presented and discussed in the chapter number four, giving a global vision of the problem. After collecting these ideas and comparing their strengths and weakness, an original architecture proposed in [12] is presented, which seems to achieve a good compromise between degree of integration and resource sharing, as well as in the derived dynamic range and speed requirements imposed to the ADC.

With the set of specifications already given, chapter number five presents the architectural design aspects of the required dual mode $\Sigma\Delta$M. Different architectural choices are analyzed and compared. Special attention is put on the resonator structures required for wide-band operation. Delay-based and integrator-based resonators were analysed in detail. The conducted study justifies the selection of the architecture in use and derives the requirements for the circuit elements necessary to construct the modulator. Circuit design issues are addressed in chapter six, here the main tasks were the election of an operational transconductance amplifier (OTA) topology

suited for high speed together with low power consumption. The design of a voltage comparator and layout design aspects are also presented.

Using a 0.35μm double-poly triple-metal N-well CMOS technology, a prototype of the already designed multi-mode modulator was fabricated. Test results and characterization of the proposed converter are the subject of the chapter number seven. There, the most significative parameters concerning mobile telecommunications are reported.

Finally, conclusions and recommended future work are presented. The key research contributions of the present work are discussed.

Chapter 2

Base-band and Intermediate Frequency Processing in Radio Receivers

Contents

2.1 Introduction

In this chapter, the receiver architectures most suited for use in mobile phone receivers are presented. They have been ordered following a historical path so that the evolution concerning the degree of integration of them can be visualized. The appearance of these reception methods has in fact marked the path to a full-integrated receiver solution. The driving forces behind the development of a single-chip radio are mainly the reduction of the fabrication costs and power consumption of the transceivers , that are important concerns for personal mobile terminals. Another aspect that has been gaining importance is the adaptability of the transceiver to manage different communications standards. By moving the ADC stage closer to the antenna, many analog functions such as filtering and separation of the in-phase (I) and quadrature (Q) components of the signal can be performed in the digital domain, where the implementation of those operations in a programmable fashion is easier. This in turn eliminates some

of the non-integrable analog components and improves the flexibility of the receiver enabling the management of multiple communications standards. The present discussion contrasts the reception methods with respect to integration, flexibility and requirements imposed to the ADC.

2.2 Superheterodyne Receiver

The superheterodyne (SH) receiver was invented in 1918 by Edwin Armstrong [15]. Since then it has been successfully used in a wide variety of applications such as home receivers for AM and FM as well as in the mobile telephony scenario. A generic SH receiver architecture is depicted in Figure 2.1. The very well known principle of filtering and mixing the incoming (usually very high frequency) signals with another signal generated within the receiver at a fixed and lower frequency, is the base of the high selectivity exhibited by this kind of receivers. However, the required quality factor of the filters involved in that process is so high, that it can only be achieved by using passive filters based on crystals, such as the surface acoustic wave (SAW) filters or ceramic filters. On the path to a full integrated receiver fabricated using low cost CMOS technologies, the presence of these elements is an unavoidable obstacle to choose the SH receiver as a candidate for the realization of a single-chip receiver [16]. The signal path of this receiver after the antenna first encounters usually a SAW filter, which selects the RF band and attenuates the out-off band blockers and interferers. The signal is amplified by means of a low-noise amplifier and the image blocker is filtered usually with a second SAW bandpass filter. Then the signal is mixed to the first fixed intermediate frequency (IF) and the desired channel is selected by means of a ceramic filter. Before quadrature down-conversion, the signal is again amplified by means of an amplifier with automatic gain control. The channel selection is finalized with integrated baseband filters and the signal is converted to the digital domain. The trade-off between sensitivity and selectivity can be improved using two or more IFs, with the added expense of extra mixer stages and extra passive image filters. Multi-mode implementation of the SH receiver would require separate analog baseband channel selection filters for different modes, in addition to a low integration level.

2.3 Direct Conversion Receiver

The direct conversion receiver, also called homodyne receiver or zero IF receiver, uses a signal coming from the local oscillator for the mixing of the desired band. The frequency of the local oscillator equals the centre of the RF band of interest plus/minus a small offset necessary to select the channel. This multiplication in time transfers the centre of the channel to be detected, directly to DC, which is equivalent to have an IF equal to zero. In the zero IF approach,

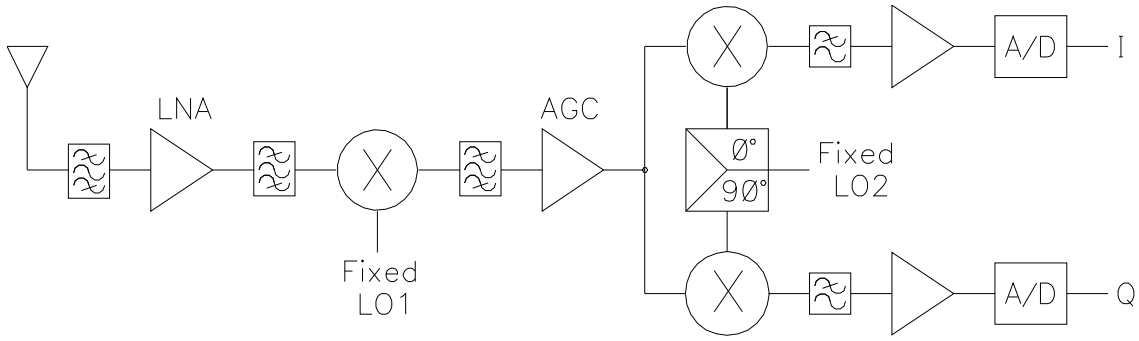

Figure 2.1: Architecture of a superheterodyne receiver

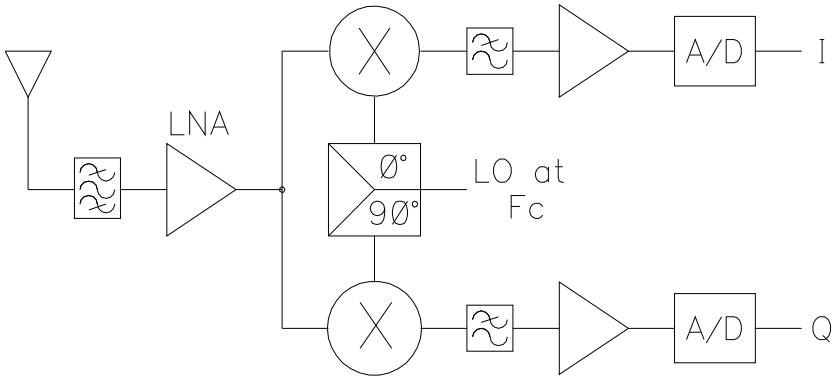

Figure 2.2: Architecture of a direct conversion receiver

quadrature mixing of the incoming signal is necessary to avoid the irrecoverable destruction of the transmitted information [17], since frequency or amplitude and phase modulated signals have a spectrum, whose negative and positive frequency components are not identical. This mixing operation with complex signals virtually eliminates the image problem present in the SH receiver. A block diagram showing such a receiver is depicted in fig. 2.2. When compared with the previous receiver, it is clear that the radio frequency front-end of a homodyne receiver is much simpler and requires less high Q crystal-based filters; in principle only the first band-selection SAW filter would be required as an non-integrable element. All other components are fully integrable using current low-cost CMOS technologies, being so a more adequate architecture for the implementation of a single-chip radio. Analog to digital conversion (ADC) takes place in this receiver earlier than in the SH counterpart, enabling so the use of reconfigurable digital hardware to operate with different communications standards. Although the advantages of the direct conversion receiver over the SH are clear, some problems appearing at the real implementation of such radios have left this architecture restricted to be used with wide-band applications like Bluetooth or WDCMA, where these penalties are less critical. These impairments are mainly: the DC offset and the mismatch of the *I* and *Q* paths. Homodyne receivers are also sensible to even order distortion, which is not a problem in a non-zero IF system. With

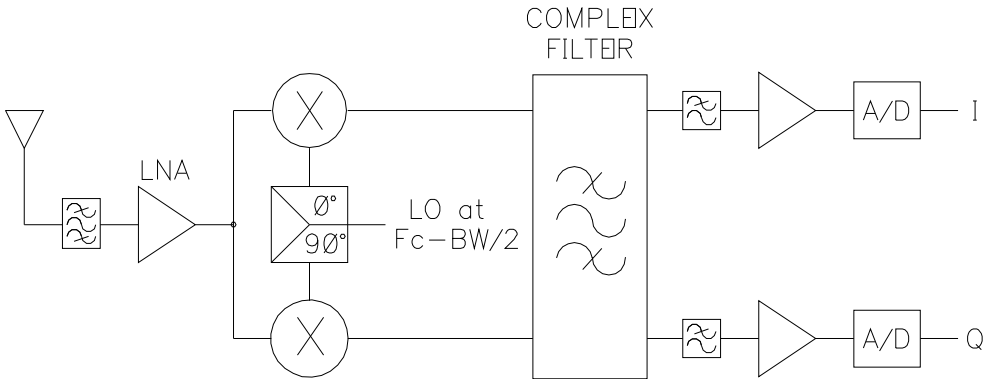

Figure 2.3: Architecture of a low IF receiver

only a low-noise amplifier and a mixer present at the RF section of this receiver, the input signal remains so weak, that the input referred noise of the base band stages becomes critical, particularly the flicker noise ($1/f$ noise) is a design issue in CMOS implementations. Finally leakage from the local oscillator to the antenna causes interferences in the band of other users. There are however, design techniques useful to reduce this problems; a good description of them can be found in [18].

2.4 Low IF Receiver

Many of the problems depicted by the zero IF approach can be significantly reduced if the resulting IF is chosen so that the DC offset effects are no longer significant but the channel to be selected remains in a frequency band low enough to be filtered by fully integrated analog filters. This is the fundamental idea behind the so-called "low IF receiver". Fig. 2.3 shows a block diagram of the architecture of a generic low IF receiver.

In this reception chain, after the RF band of interest has been selected by a band pass SAW filter and amplified by a low noise amplifier, it is mixed in quadrature with the signal coming from the local oscillator. The frequency of the local signal is often chosen to be equal to the centre of the desired band minus a frequency offset one half, once or twice smaller than the band width of the channel to be detected. The complex mixing operation centres the wanted signal around the positive component of the low IF value and the image signal is centred around the negative component. This fact makes necessary the use of a complex filter for image rejection. However, because of the lower value of the chosen IF such filters are fully integrable, both in passive or active fashion, using current low cost CMOS technologies[19],[20]. Multimode operation of this architecture would require that these filters were replicated for each standard, because they perform the channel selection in the analog domain.

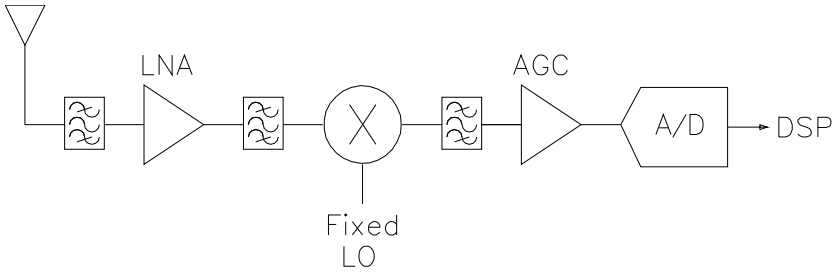

Figure 2.4: Architecture of a digital IF receiver

2.5 Digital IF Receiver

Programmable filters aimed for the selection of the desired channel are an important requirement for the successfull implementation of a multistandard receiver. Filtering operations with programmable characteristics are much more easily realized in the digital domain. The fixed analog channel selection performed in the SH receiver has a disadvantage in that it cannot process multistandards and multichannels. These facts have been the driving force behind the extensive research in the developing of a receiver with digitization at the IF stage, which is the idea of the so-called digital IF receiver. In the digital IF receiver architecture, digitization is moved up from baseband to IF, thereafter, and digital signal processing techniques are used to recover the transmitted signal. The digital signal processing techniques used include direct digital frequency synthesis, digital down conversion, digital filtering and multirate techniques such as decimation and interpolation. Fig. 2.4 shows a typical architecture of a digital IF receiver.

In spite of the mentioned advantages, this architecture has not been used in real mobile communications equipment mainly because of the limitations of current ADC implementations. Due to the minimum analog signal processing present in the reception chain, the desired signal remains so weak at the input of the ADC, that its required linearity, dynamic range and noise floor have been unreachable with current technologies using a reasonable power consumption [2]. For those reasons this architecture as well as the development of ADC's capable to satisfy the imposed requirements are still subject of intensive research [21], as mentioned above.

2.6 Summary

This chapter presented a brief description of the receiver architectures that have been used in the mobile telephony. The discussion has contrasted the reception methods regarding their flexibility and performance imposed to the ADC. For a deeper study of the presented receivers the reader should be submitted to [2] or [13]. As it has been pointed out, a very important

Receiver Architecture	Degree of Integration	Multistandard Capabilities	ADC Design
Superheterodyne	Low	Low	Simple
Homodyne	High	High	Difficult
Low IF	High	Medium	Difficult
Digital IF	High	High	Very Difficult

Table 2.1: Comparison of the integration and multistandard capabilities of the discussed receiver architectures

characteristic of a radio receiver architecture aimed for multimode operation is programmable filtering for channel selection. In this sense, the best candidates to be chosen as basis for the development of a multistandard mobile terminal are the Zero IF and the Digital IF architectures. The weakness of both architectures have already been discussed, being those of the digital IF so, that its application in a real mobile phone has to wait until the appearance of an ADC able to fulfil the imposed requirements. On the other hand, Zero IF receivers have already been used in wide-band applications using certain circuit techniques to overcome its impairments. Thinking about the current necessity of managing narrow- and wide- band signals, a possible solution to the problem could consist of the Zero IF approach together with an appropriate reception method for narrowband signals. A natural way would be the usage of the Low IF architecture because of their similitude. These topics are going to be discussed in detail until the chapter number 4, where the already developed methods for multistandard reception are presented together with the proposed approach. We conclude this chapter with table 2.1, where the main characteristics of the discussed receiver architectures are summarized and compared.

Chapter 3

Sigma Delta Modulator Fundamentals

Contents

3.1 Introduction

Conversion of real world analog signals into their digital representation enables efficient transmission and storage of digital signals. This in turn also permits the intricate processing of the signal, which is only feasible in the digital domain with the use of microprocessors or digital signals processors. The reconstruction of the original signal is also a requirement in order to have an understandable signal for the final user. These important signal transformations are accomplished by an ADC and a Digital to Analog Converter (DAC), respectively. Digital Systems have been strongly benefited by the continuous scaling of CMOS technology during the last three decades [22]. This aggressive scaling has mainly bestowed digital systems with the benefits of smaller devices, such as increased transistor density, gate speeds on the order of tens of picoseconds and reduced threshold voltage (V_T), which are reflected in an increased arithmetic and logic synthesis capacity, higher speed of operation and lower power consumption. This is unfortunately not the case for analog systems, and analog circuit designers are currently faced with problems that emerge from using a fabrication process optimized for digital circuits. Short channel effects appearing in current sub-micrometric devices bring as a consequence a reduction of the intrinsic voltage gain ($g_m r_O$) of CMOS amplifiers, matching of these elements is also poor, which together with a reduced power supply voltage limit the achievable dynamic range of Nyquist-Rate ADC architectures. It is possible to achieve a high dynamic range in spite of the poor analog device behaviour present in modern VLSI processes, through the usage of oversampling, feedback, and digital filtering. These are the basics of the ΣΔ ADC's. This chapter addresses the principles of the analog to digital conversion both in oversampled and Nyquist-rate methods. The theoretic description given here intends to clarify the limitations of Nyquist-rate converters as well as the advantages obtained, at the system level, by using noise shaping techniques joined with oversampling. The idea of shaping the quantization noise around DC, better known as ΣΔ modulation is explained and quantitatively analyzed. Besides its robustness against analog circuit imperfections, ΣΔM's have an excellent tonal behavior which is reflected in a large SFDR. This is a very desirable characteristic for wireless communications, which is also treated in this chapter. Noise suppression at certain frequency achieved by BPΣΔ is presented and analized as well.

3.2 Nyquist Rate Analog to Digital Converters

An ADC performs over its input signal a non-linear, non-reversible process, because an infinite number of input amplitude values are mapped to a finite number of output amplitude values. The quantized output amplitudes are represented by a digital code word composed of a finite number of bits. Depending on the application, this number of bits could be a low-resolution

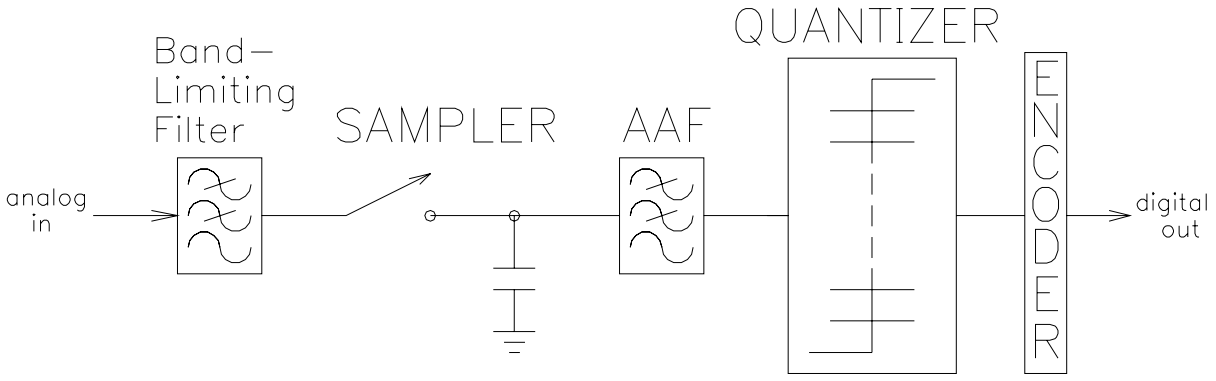

Figure 3.1: Basic operations involved in A/D Conversion

representation of just 4 bits or a high-resolution representation with more than 16 bits. The basic operations involved in A/D conversion are shown in Figure 3.1.

The analog input signal, $x(t)$, first encounters an "anti-alias" filter (AAF), which removes the signal components above one-half of the sampling rate of the subsequent sampler. This filter is necessary because according to the Nyquist sampling theorem [23], high frequency components of $x(t)$ would alias into the passband upon sampling, causing distortion that cannot be filtered or even distinguished from the original signal. Following the AAF, the bandlimited signal, $x_a(t)$, is sampled, thus yielding the discrete-time signal, $x_s(t) = x_a(nT_s)$, which is still continuous in amplitude. The sampled-data analog signal is then discretized in magnitude by the ensuing quantizer before being encoded into the output data signal, $y[n]$.

3.2.1 Sampling

The Nyquist sampling theorem establishes the minimum number of samples, that a band-limited signal should contain in the time domain, if there is to be no loss of information or aliasing distortion by recovering the sampled signal. According to that, $x(t)$ must be sampled at a frequency higher than twice the baseband cutoff frequency, f_b, which is defined as the cutoff frequency for the antialiasing filter as shown in Figure 3.2. In the frequency domain, the spectrum of the sampled signal, $x_s(t)$, is

$$X_s(f) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} X_a(f - k f_s) \tag{3.1}$$

If the sampling frequency, f_s, is chosen to be at, or slightly higher than, the Nyquist rate, $2 \cdot f_b$, then the converter is said to be a *Nyquist-rate converter*. However, the sampling rate

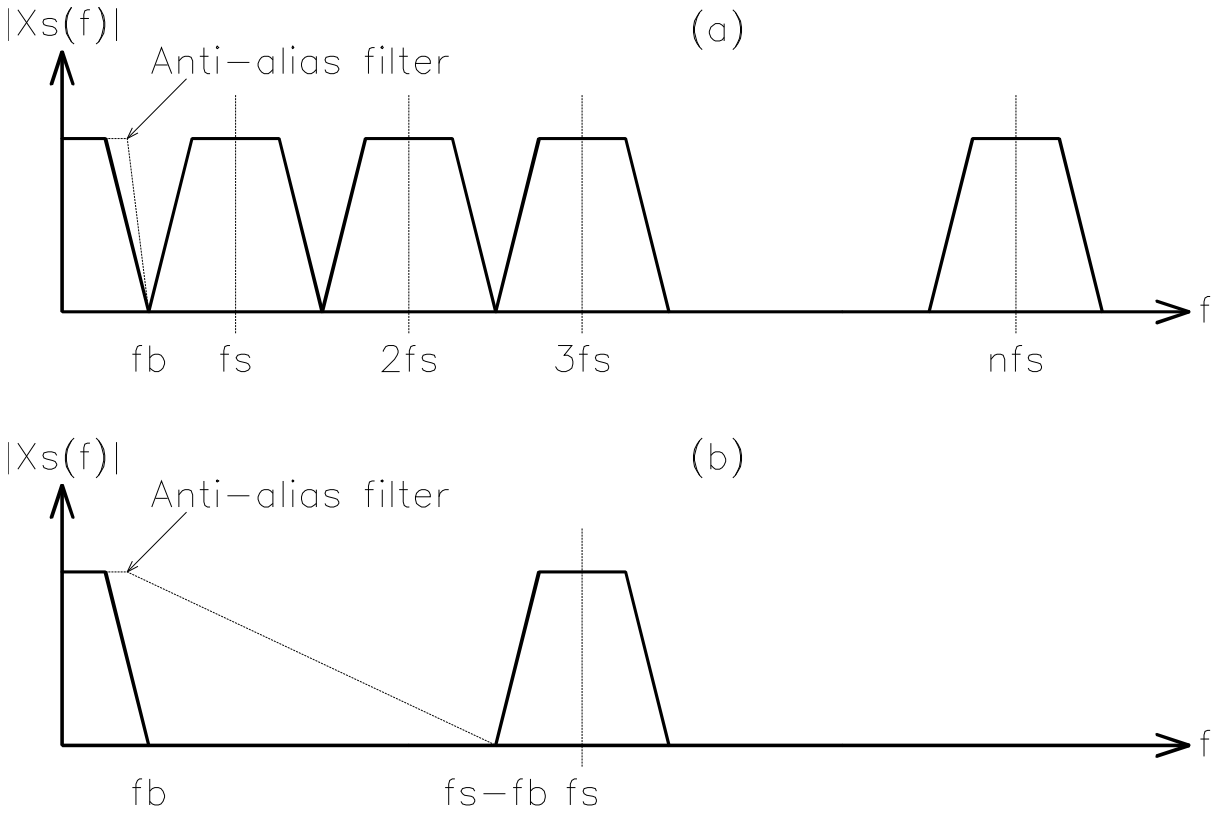

Figure 3.2: Spectrum of a band-limited signal (a) sampled at the Nyquist rate, and (b) oversampled

can deliberately be chosen to greatly exceed the Nyquist rate in order to exploit the benefits of oversampling, to be described later in this chapter. In this case, the converter is referred to as an *oversampling converter*. When the passband extends from DC to f_b, the oversampling ratio, (*OSR*), is defined as $OSR = f_s/(2 \times f_b)$, with *OSR* = 1 for a Nyquist-rate converter. These two kinds of sampling are shown in Figure 3.2.

3.2.2 Quantization

In principle, the sampling process does not result in any loss of information, after meeting the requirement that the sampling rate equals or exceeds the Nyquist rate. However, this is not true for the quantization of the sampled signal because, in this non-reversible operation a continuous range of amplitudes is mapped into a finite set of digital output codes. The transfer characteristic of a uniform quantizer with a gain of unity is presented in Figure 3.3(a), and the resulting sawtooth quantization error is illustrated below in Figure 3.3(b). A unity-gain, uniform N-bit quantizer has 2^N quantization levels, and the step size, Δ, between quantization levels is

$$\Delta \doteq \frac{V_{REF}}{2^N - 1} \tag{3.2}$$

where V_{REF} is the full-scale input and output range of the quantizer.

The output of the quantizer can be written as a sum of the input signal, $x[n]$, with the quantization error, $e[n]$, which is the result of a nonlinear operation, $q\{\cdot\}$, on $x[n]$:

$$y[n] = x[n] + e[n] = x[n] + q\{x[n]\} \tag{3.3}$$

Analyzing the effects of the quantization errors using this non-linear, signal dependent model can conduct to intractable equations. The analysis can be simplified if the non-linear quantization noise is modeled as an additive white noise source and the study is carried out using statistical methods. This statistical representation of the quantization errors is based in the following assumptions [23]:

1. the error sequence $e[n]$ is a sample of an stationary random process.
2. the error sequence is not correlated with the input sequence $x[n]$.
3. the random variables of the quantization process are not correlated. That means, quantization is a white noise process.
4. the probability distribution of the error process is uniform

After the given assumptions, the quantization error, $e[n]$, has a probability density function with a rectangular shape, as shown in the Figure 3.4.

With this, the quantizer can be replaced with the linear stochastic model presented in Figure 3.5, $e[n]$ has a power or variance given by:

$$\sigma_e^2 = \int e^2 p_E(e) de = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{3.4}$$

This value enables us to calculate the *signal-to-quantization noise ratio* (*SQNR*) for an N bit ADC, which is defined as the ratio of the input signal power, σ_x^2, to the variance of the quantization noise, σ_e^2. If the input signal is a sinusoid of amplitude A whose power is $\frac{A^2}{2}$, after 3.2 and for a large N we have: $\Delta \approx \frac{V_{REF}}{2^N}$; thus:

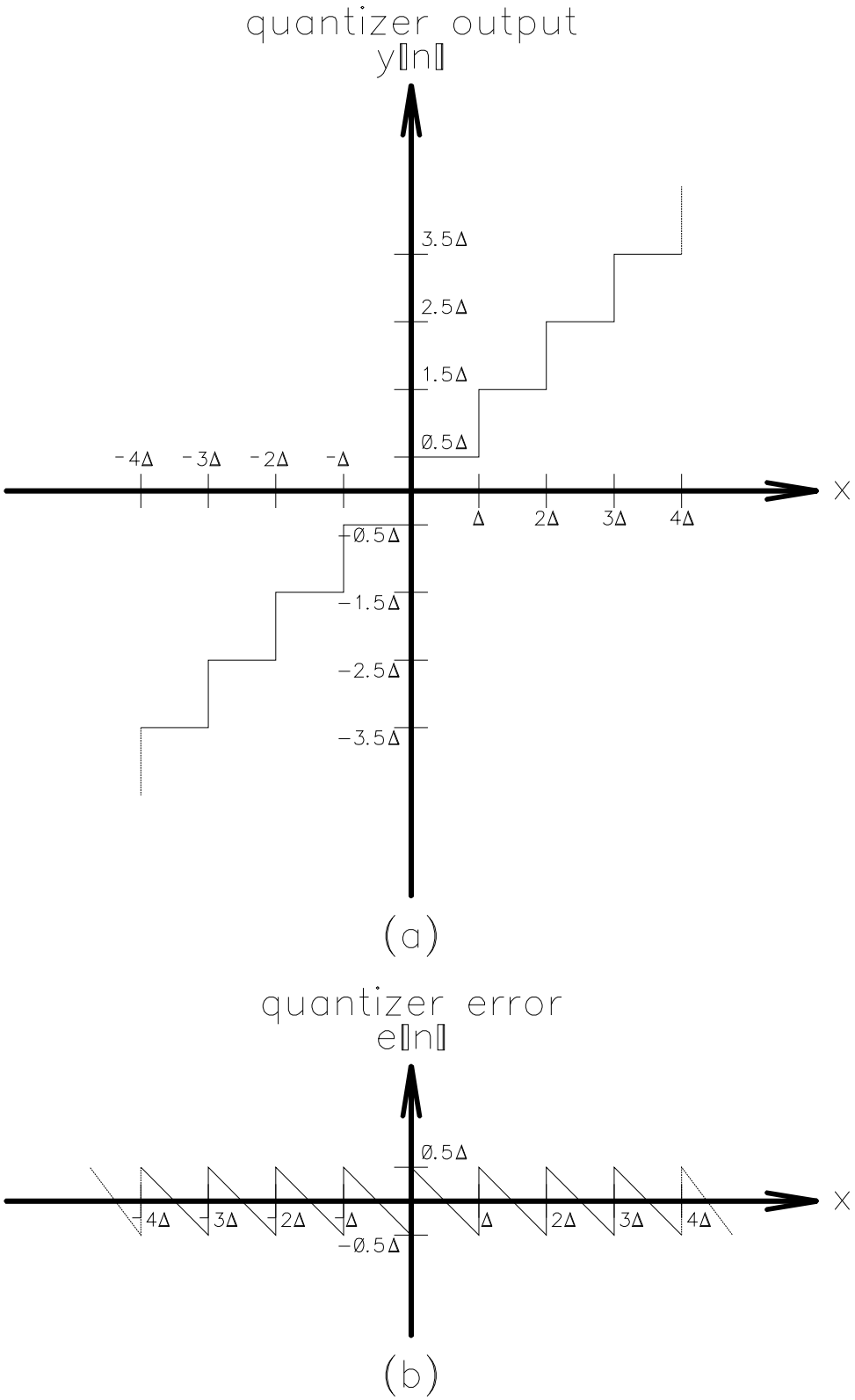

Figure 3.3: Transfer (a) and error (b) characteristics of a uniform quantizer

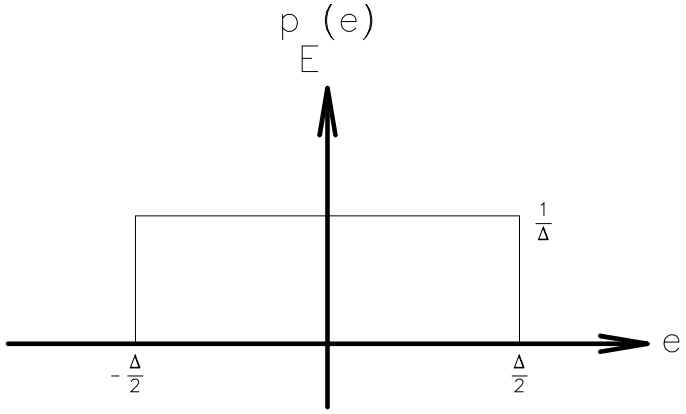

Figure 3.4: Probability density function of $e[n]$

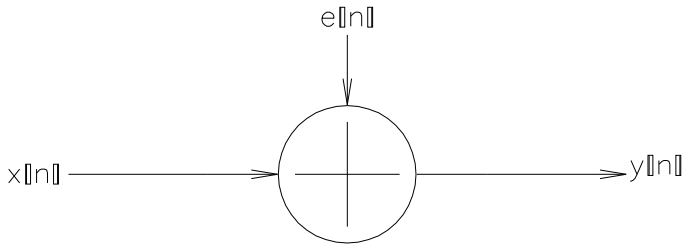

Figure 3.5: Linearized, stochastic model of the quantizer

$$SQNR = 10\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) = 10\left(2N\log 2 + \log 6 + \log\frac{A^2}{V_{REF}^2}\right)$$
$$= 6.02N + 7.7 + 10\log\frac{A^2}{V_{REF}^2} \tag{3.5}$$

The *dynamic range of an ADC,* (DR) is defined as the ratio of a full scale input signal power to the power of an input signal level that yields a signal-to-noise ratio of one. Given that a N-bit quantizer has 2^N quantization levels, a full-scale sinusoidal input to the quantizer has an amplitude of $2^{N-1}\Delta$ and a corresponding signal power of $2^{2N-3}\Delta^2$, if the noise floor of the ADC is determined primarily by quantization noise, the *DR* equals to:

$$DR = 10\log\left(\frac{\sigma_x^2}{\sigma_e^2}\right) = 10\log\left(\frac{2^{2N-3}\Delta^2}{\frac{\Delta^2}{12}}\right) = 6.02\times N + 1.76dB \tag{3.6}$$

Therefore, if the resolution of an ADC is limited by quantization noise, then its *SQNR* and *DR* increases by approximately 6 dB with every additional bit of resolution. In practical implementations, the minimum resolvable signals may be limited by circuit noise or thermal noise rather

than quantization noise. Nevertheless, in such cases, the *DR* is defined similarly with the lower limit established by an input signal level that yields a signal-to-noise ratio of one.

3.2.3 Limitations of the Additive White Noise Model

In many cases in this research, the nature of the input signal and the quantizer violate one or more of the assumptions needed to justify the modeling of the quantizer as a source of additive white noise. Duet to the correlation of the quantization noise with the input signal, the spectrum of the quantizer output can contain discrete tones that are not predicted by the white noise model [24]. This correlation is particularly strong in the case of the two-level or 1-bit quantizers used in the feedback modulators to be described later in this chapter. However, it is nevertheless useful to model the quantizer in this manner to predict the performance of an A/D converter, despite the failure of the system to adhere to the stipulations of the model. In particular, even though the 1-bit quantizer violates the conditions of the model, the white noise quantizer model still allows for an accurate estimate of the dynamic range of a modulator that is comprised essentially of a 1-bit quantizer embedded in a feedback loop. In such cases, the only justification for modeling the quantizer as an additive white noise source is that behavioral simulations of the system confirm the estimate of the dynamic range arrived at with the use of this model.

3.2.4 Limitations of Nyquist-Rate ADC's

There are many architectures for Nyquist-rate A/D converters, each of which embodies various tradeoffs among bandwidth, power dissipation, area, and dynamic range requirements. A thorough review of many architectures is presented in [25], [26]. A common limiting factor in all Nyquist-rate architectures is that some operations such as comparison, amplification or substraction must be performed to the overall precision of the converter. This typically translates into the need for precise component matching unless special calibration, error-correction or trimming techniques are used, with attendant penalties in the area, power dissipation or manufacturing cost. With careful layout techniques, matching of 0.3% can be routinely achieved in modern CMOS processes, and matching as good as 0.1% has been observed [27]. However, it is important to note that even with 0.1% matching, the resolution of an uncalibrated and untrimmed Nyquist-rate converter is limited to only 10 bits. A steep AAF must also precede any Nyquist-rate ADC. This bandlimiting filter rejects frequency components of the signal located above one-half of the sampling frequency in order to prevent aliasing distortion. However, to allow for a large signal bandwidth, the stopband corner frequency of the filter must also be near $f_s/2$. Thus, as depicted in Figure 3.2(a), the AAF must have a sharp transition band, which typically introduces phase distortion in signal components located near the cutoff frequency. Furthermore, it is difficult to implement precise analog filters with multiple poles in a VLSI

technology due to a lack of high-Q inductors and well-defined, stable resistor and capacitor values. Circuit noise and distortion in active implementations of continuous-time filters, such as g_m/C topologies, often limit their utility to applications that only require a low- to medium dynamic range [28], [29]. This becomes increasingly true at the low supply voltages, 2.5 V to 3.3 V, typical of submicron technologies, in which the large signal swings necessary for a high dynamic range directly conflict with the linearity requirements of the filter. Finally, the precisely defined poles and zeros of any high-order continuous time filter will be subjected to a wide range of environmental and processing fluctuations that can potentially disturb the pass-band response and degrade the sharp selectivity of the filter. Thus, a compensatory automatic tuning scheme may be necessary to constrain the variations of the frequency response of the filter [29].

3.3 Oversampled Analog to Digital Converters

By exploiting the speed of a VLSI technology, it is often possible to sample the input signal at a rate much higher than the Nyquist rate. This oversampling offers the immediate advantage of relaxing the requirement for a steep transition band on the AAF, as illustrated in Figure 3.2(b). However, as discussed in the following section, oversampling by itself leads to only modest improvements in resolution of the converter. If the quantizer is also embedded in a feedback loop, it is possible to significantly increase the resolution of a converter beyond what can be achieved simply by oversampling. It is important to note that the quantization process in an oversampled converter employing feedback differs fundamentally from that in a Nyquist-rate converter. It is not necessary to quantize the signal in an oversampled converter to the full resolution of the converter, since each sample of the input signal correspond to more than one output sample. Rather, in the digital filter that follows the oversampled converter, many coarsely quantized samples are processed to yield a more precise estimate of the analog input signal at a lower sampling rate. Thus, each output sample depends on a long sequence of input samples. In many cases, single-bit quantization is sufficient in an oversampled feedback modulator.

3.3.1 Oversampling

The resolution of a Nyquist-rate converter can be increased in a straightforward manner by operating the converter at a sampling rate in excess of the Nyquist rate. As found in Section 3.1.2, if the quantization error is modeled as an additive white noise source, the total noise power, $\Delta^2/12$, is uniformly distributed across the sampling bandwidth from -$f_s/2$ to $f_s/2$ with a power spectral density N_e of:

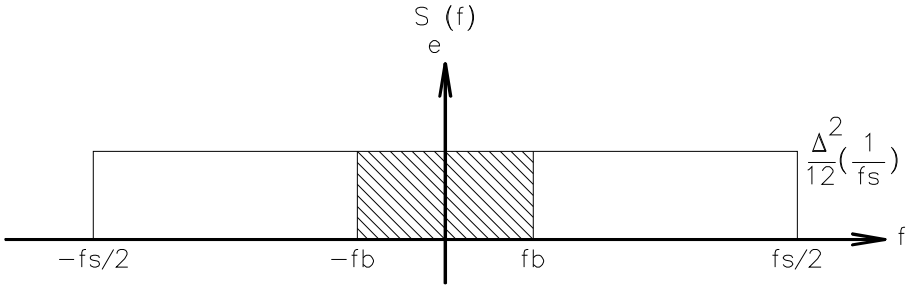

Figure 3.6: Power spectral density of quantization noise when the input signal is oversampled.

$$N_e = \frac{1}{f_s} \times \sigma_e^2 \tag{3.7}$$

When the input is oversampled, the signal bandwidth extends form -f_b to f_b and is only a fraction of the sampling bandwidth, as depicted in Figure 3.6. Therefore, if the desired signal band is ideally filtered by a digital filter (H_d), the in-band noise power in the presence of oversampling is:

$$\sigma_e^2 = \int_{-f_b}^{f_b} |H_d(f)|^2 N_e df = \frac{\Delta^2}{12} \times \frac{2 \times f_b}{f_s} = \frac{\sigma_e^2}{OSR} \tag{3.8}$$

Thus, the quantization noise power, σ_e^2, is reduced by a factor $1/OSR$, and the maximum achievable dynamic range increases by 3 dB, or 1/2 bit, per octave of oversampling. This is valid for all ADCs but further noise reduction is possible by quantization noise shaping, which is utilized in ΣΔM's.

3.4 Lowpass Sigma Delta Modulation

3.4.1 Feedback Modulators

The general structure of a feedback modulator is illustrated in Figure 3.7, which shows a quantizer embedded in a loop with a DAC in the feedback path. The transfer function of the filter in the forward path of the modulator is denoted $A(z)$, while the filter in the feedback path has the transfer function $F(z)$. If the quantizer represented in figure 3.7 is substituted with the linear model of figure 3.5 the linear system depicted in figure 3.8 is obtained. For this last system the output of the resulting linearized feedback modulator is described in the z-domain by

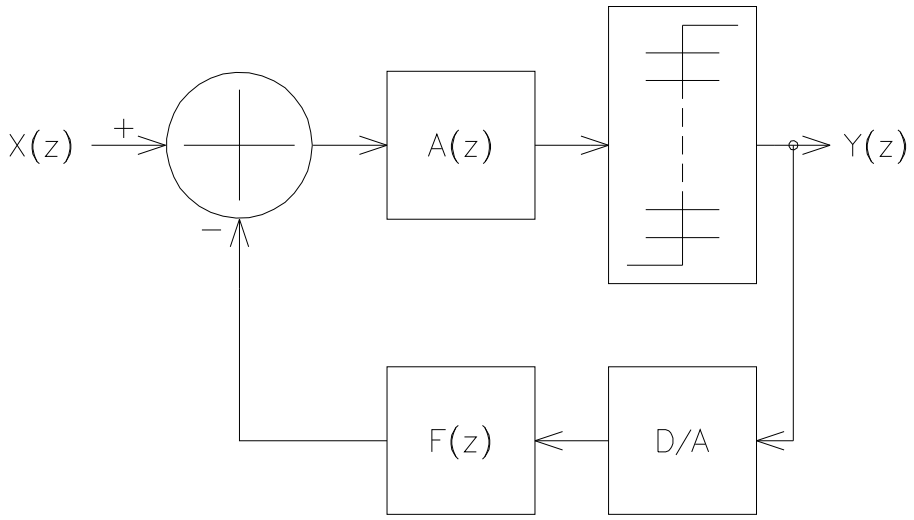

Figure 3.7: General structure of a feedback modulator.

$$Y(z) = \frac{A(z)}{1+A(z)F(z)} \times X(z) + \frac{1}{1+A(z)F(z)} \times E(z) \tag{3.9}$$

Feedback modulators [30] are commonly described in terms of two broad classes based on the characteristics of the forward-path and feedback-path transfer functions. In predictive modulators, the feedback filter, $F(z)$, has a large gain in the signal passband and provides an estimate of the input signal, which is then subtracted from the actual input to the modulator, $X(z)$. If the predicted value is close to the input value, the quantizer input will be small, allowing the use of a quantizer with a small input range. In effect, by encoding the rate of change of a signal rather than the signal itself, a predictive modulator can employ a quantizer with a small step size and a commensurately small quantization error. In contrast, noiseshaping modulators do not reduce the magnitude of the quantization noise. Instead, a large frequency-dependent gain in the forward path, $A(z)$, is used to spectrally shape the quantization noise and suppress it in the signal passband. Most of the power in the quantization noise is moved into the stopband where it is removed by a digital filter that follows the modulator. In a predictive modulator, both the input signal and the quantization noise undergo spectral shaping. This fact has important implications in the practical implementation of feedback modulators. From (3.8) it is seen that the *signal transfer function*, $(STF(z))$, of a feedback modulator is:

$$STF(z) = \frac{A(z)}{1+A(z)F(z)} \tag{3.10}$$

Since the passband gain of the feedback filter, $F(z)$, is very high in a predictive modulator, the signal transfer function is approximately $1/F(z)$. Therefore, the digital filter that follows

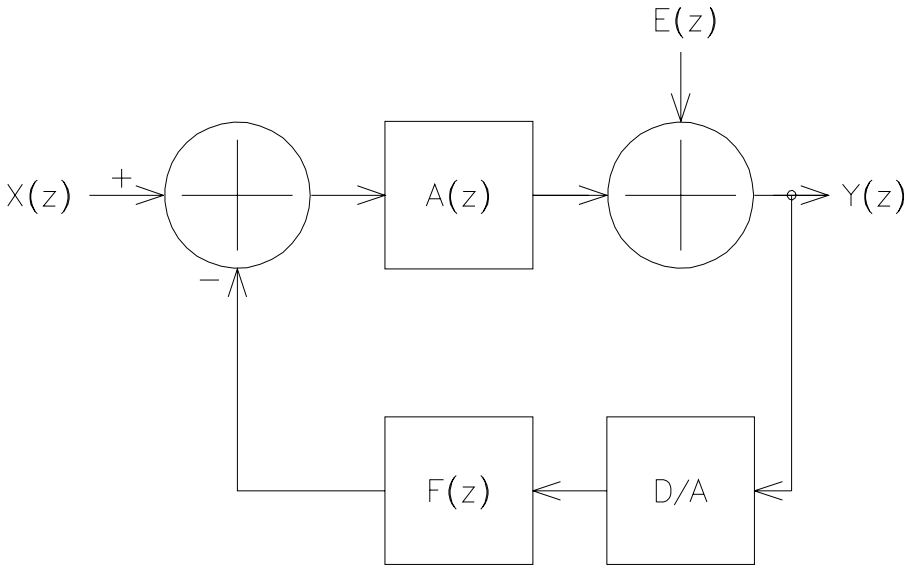

Figure 3.8: Linearized model of a feedback modulator.

a predictive modulator must apply an inverse transfer function, $\hat{F(z)}$, which is a digital approximation of the analog feedback filter transfer function $F(z)$, to the output of the modulator in order to recover the input signal. Mismatch between $\hat{F(z)}$ and $F(z)$ presents an immediate limitation because the non-idealities in the analog circuits that are the root cause of the mismatch cannot be predicted a priori. Furthermore, mismatch-related errors are greatly amplified because the passband gain of $F(z)$ is very high. In noiseshaping modulators, only the quantization noise is spectrally shaped. The forward filter, $A(z)$, has a large passband gain and the feedback filter, $F(z)$, is independent of frequency in the passband. Therefore, the signal transfer function, (3.9), reduces to a constant in the passband, and the digital filter that follows a noiseshaping modulator must only reject the large, out-of-band quantization noise without altering the frequency response in the signal passband. The performance of a noiseshaping modulator is not limited by the need to match a digital decoding filter to the analog feedback filter, $F(z)$, in the modulator. For this reason, noiseshaping topologies are preferred if the feedback modulator is to be implemented with analog circuitry. This research work focuses exclusively on noiseshaping topologies. At this point, it is important to note that in the development of noiseshaping techniques it was usually presumed that the signal passband was situated at baseband. However, spectral shaping of noise is not restricted to the lowpass domain. Rather, through an appropriate choice of the forward and feedback transfer functions, $A(z)$ and $F(z)$, it is possible to shape the bulk of the quantization noise power away from any region in the sampling bandwidth, -$f_s/2$ to $f_s/2$. The concept of bandpass noiseshaping will be developed later in this chapter following the initial discussion of lowpass noiseshaping.

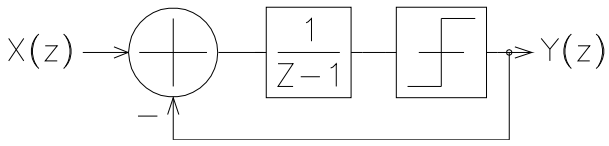

Figure 3.9: First order lowpass ΣΔM.

3.4.2 First Order Sigma Delta Modulator

In noiseshaping topologies, the forward path filter is designed to have a large gain in the passband in which the quantization noise is to be suppressed. From Figure 3.8, it follows that if $F(z)$ is chosen to be 1, the z-domain expression for the output can written as

$$Y(z) = \frac{A(z)}{1+A(z)}X(z) + \frac{1}{1+A(z)}E(z) \tag{3.11}$$

where $X(z)$ and $E(z)$ are the z-transforms of the input signal and quantization error, respectively. Therefore, if the quantization noise is to be suppressed in the baseband, $A(z)$ must have a large DC gain. There are many transfer functions that satisfy this condition and could be used to implement a noiseshaping modulator, but one class of transfer functions comprised of integrators is especially suited for VLSI implementation because the analog circuits required to implement the transfer function are simple and robust. A z-domain representation of a first-order ΣΔM is depicted in Figure 3.9. The modulator is comprised of a subtraction node, a discrete-time integrator, and a 1-bit quantizer.

The integrator ideally provides an infinite gain at DC, which, from (3.11), is necessary to suppress the quantization noise at baseband. The quantization noise is injected by the comparator, which can be substituted for the model presented in figure 3.5 for the analysis, although, as mentioned, single bit quantizers strongly violates the assumptions of the additive white noise model, it is useful to take that model for an early estimation of the main performance parameters of the ΣΔM when it is used as an ADC. Refinements made on the value of the estimated data or extraction of other performance parameters such as SFDR can be done later on by means of *Behavioral Simulations* performed on the system depicted in fig. 3.9. After substituting the comparator by a white noise additive source, the representation of the first order ΣΔM is shown in the figure 3.10, which can be treated as a linear two-input one-output system.

The output in the z-domain of the system presented in fig. 3.10 is equal to:

$$Y(z) = \frac{1}{z}X(z) + \frac{z-1}{z}E(z) = X(z)z^{-1} + E(z)(1-z^{-1}) \tag{3.12}$$

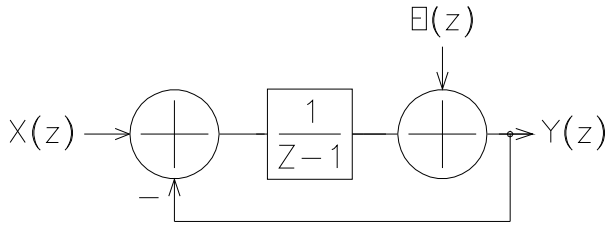

Figure 3.10: Linearized first order lowpass ΣΔM.

From the last equation the *Noise Transfer Function* (NTF) can be identified to be $(1-z^{-1})$ and the STF as z^{-1}. The signal is only delayed by a clock period. The quantization noise power spectral density (N_e) is shaped by the NTF, which has one transmission zero at 1 in a normalized discrete time frequency axis, suppressing so the quantization noise power around DC. The in-band quantization noise power P_e can be calculated by making $z = \exp(2\pi j f/f_s)$ and after that, integrating the output power spectral density within (f_b):

$$P_e = \int_{-f_b}^{f_b} \left|1-z^{-1}\right|^2 N_e df = \int_{-f_b}^{f_b} |1-\exp(-2\pi j f/f_s)|^2 \frac{\Delta^2}{12 f_s} df = \int_{-f_b}^{f_b} (2\sin(\pi f/f_s))^2 \frac{\Delta^2}{12 f_s} df \tag{3.13}$$

The out-of-band quantization noise is assumed to be rejected by a ideal lowpass digital filter that follows the modulator. Since $f_b << f_s$, the integral can be evaluated under the approximation $\sin(x) \approx x$ to yield an inband quantization noise power equal to

$$P_e = \int_{-f_b}^{f_b} \left|1-z^{-1}\right|^2 N_e df \approx \left(\frac{\pi^2}{3}\right) \times \left(\frac{1}{OSR^3}\right) \times \frac{\Delta^2}{12} \tag{3.14}$$

From 3.14 and assuming that the modulator input is a sine wave of amplitude $A \leq \Delta/2$ the *SQNR* and *DR* are given by:

$$SQNR = \frac{A^2}{2P_e} = \frac{18 \times OSR^3 \times A^2}{\pi^2 \Delta^2} \tag{3.15}$$

$$DR = \frac{(\Delta/2)^2}{2P_e} = \frac{9 \times OSR^3}{2\pi^2} \tag{3.16}$$

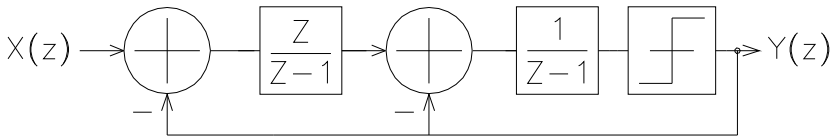

Figure 3.11: A second order lowpass ΣΔM.

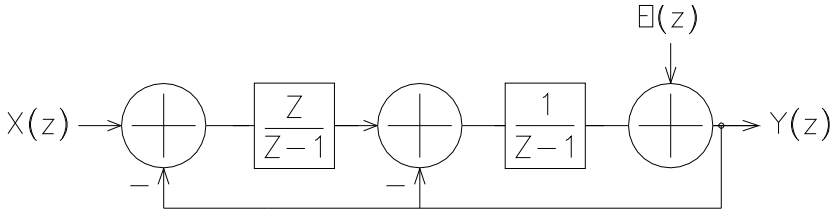

Figure 3.12: Linearized second order lowpass ΣΔM.

These relationships show that the resolution and dynamic range of the first order noise differencing ΣΔM increase with *OSR* at a ratio of 1.5 bit per octave. Although an improvement of 1 bit in *SQNR* and *DR* is observed in the 1st order ΣΔM when compared with the performance of an ADC using only oversamplig, the required f_s could still being very high for certain applications. As an example, the digitization of a GSM channel with $f_b = 200$KHz with a $SQNR = 96$dB or 16 bits would require after (3.15) an OSR around 1297, which produces a $f_s \approx 519MHz$ this is a very high sampling frequency that could compromise the power consumption in a circuit implementation of the modulator in fig. 3.9. An efficient way to reduce the required *OSR* for a given *SQNR* is to increase the order of the modulator as it is analyzed in the next subsection.

3.4.3 Second Order Sigma Delta Modulator

The architecture of a second order ΣΔM is shown in fig. 3.11. As it is seen, it comprises two integrators, the first is a "non-delayed" and the second is a "delayed" integrator.

The analysis of this modulator can be treated in the same way as with the previous one. The single bit quantizer can be substituted with an additive white noise source as it is depicted in fig. 3.12 and after that, finding out an expression for the output in the *z*-domain. Performing the mentioned steps leads to the following equation for $Y(z)$:

$$Y(z) = \frac{1}{z}X(z) + \frac{(z-1)^2}{z}E(z) = X(z)z^{-1} + E(z)(1-z^{-1})^2 \tag{3.17}$$

In this case the NTF has two transmission zeroes at DC. The in-band P_e can be found proceeding in the same way as for the first order loop:

$$P_e = \int_{-f_b}^{f_b} \left|(1-z^{-1})^2\right|^2 N_e df = \int_{-f_b}^{f_b} \left|(1-\exp(-2\pi j f/f_s))^2\right|^2 \frac{\Delta^2}{12 f_s} df = \int_{-f_b}^{f_b} (2\sin(\pi f/f_s))^4 \frac{\Delta^2}{12 f_s} df \approx \left(\frac{\pi^4}{5}\right) \times \left(\frac{1}{OSR^5}\right) \times \frac{\Delta^2}{12} \tag{3.18}$$

Similarly, if the input signal to this modulator is a sinus of amplitude $A \leq \Delta/2$ the *SQNR* and *DR* are found to be:

$$SQNR = \frac{A^2}{2P_e} = \frac{30 \times OSR^5 \times A^2}{\pi^4 \Delta^2} \tag{3.19}$$

$$DR = \frac{(\Delta/2)^2}{2P_e} = \frac{15 \times OSR^5}{2\pi^4} \tag{3.20}$$

Equations (3.19) and (3.20) show that for a second order noise differencing ΣΔM the *SQNR* and *DR* increase at a ratio of 2.5 bit per octave of *OSR*. Taking the example of the last sub-section, the digitization of a GSM channel with a *SQNR* of 96dB would require an *OSR* on the order of 106, that means $f_s = 42.4MHz$, which is a much more realistic value reachable in current CMOS technologies without putting in risk the low power constraints imposed by the mobile communications equipment. As it can be observed, augmenting the order of a ΣΔM reduces the required *OSR* in order to reach a given *SQNR*. This intuitively leads to the supposition that using high-order noise differencing loops is the way to have high *DR* with moderate f_s. In the next section a brief analysis and discussion of a *n*-order ΣΔM is presented.

3.4.4 *n*-Order Sigma Delta Modulator

A conceptual architecure of a *n*-order ΣΔM that produces a quantization noise differencing of order *n* is presented in figure 3.13. Here, the first $n-1$ integrators are non-delayed and the last one is a delayed integrator. The single bit quantizer introduces the quantization noise and could also be substituted by the linear stochastic model of fig. 3.5. It can be demonstrated that the output of such a system equals to:

$$Y(z) = \frac{1}{z}X(z) + \frac{(z-1)^n}{z}E(z) = X(z)z^{-1} + E(z)(1-z^{-1})^n \tag{3.21}$$

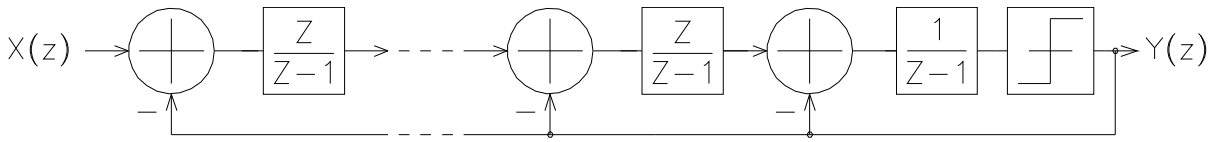

Figure 3.13: A $n-$order lowpass ΣΔM.

Using the former procedure and approximation, the in-band P_e for an n-order lowpass ΣΔM can be found:

$$P_e = \int_{-f_b}^{f_b} \left|(1-z^{-1})^n\right|^2 N_e df = \int_{-f_b}^{f_b} \left|(1-\exp(-2\pi j f/f_s))^n\right|^2 \frac{\Delta^2}{12 f_s} df = \int_{-f_b}^{f_b} (2\sin(\pi f/f_s))^{2n} \frac{\Delta^2}{12 f_s} df \approx \left(\frac{\pi^{2n}}{2n+1}\right) \times \left(\frac{1}{OSR^{2n+1}}\right) \times \frac{\Delta^2}{12} \tag{3.22}$$

Doing the same assumptions for the input signal leads to the following expressions for the *SQNR* and *DR*:

$$SQNR = \frac{A^2}{2P_e} = \frac{6 \times (2n+1) \times OSR^{2n+1} \times A^2}{\pi^{2n}\Delta^2} \tag{3.23}$$

$$DR = \frac{(\Delta/2)^2}{2P_e} = \frac{3 \times (2n+1) \times OSR^{2n+1}}{2\pi^{2n}} \tag{3.24}$$

Using the same example as for the first and second order loops, but now taking a 4th-order modulator, the required *OSR* to produce a *SQNR* of 96 dB is found to be around 22, equivalent to a $f_s = 8.8MHz$ with $f_b = 200KHz$ as established for GSM signals. The graphic number 3.14 shows the frequency response of the NTF for noise differencing loops of 1st-, 2nd- and 4th-order.

It is interesting to note how the gain of each NTF increases at πrad/s $(f/f_s = 1/2)$ as the order of the modulator augments. This out of band gain is the root of the instability observed in high order ΣΔMs that uses a pure differencing transfer function for their noise shaping and whose architecture is based on the direct extension of the first order loop as shown in fig. 3.13. There is however a method to design stable single bit ΣΔMs with order higher than two, whose architectures are based on modifications performed over the generic topology of fig. 3.13. Those architectures as well as the design methodology used to stabilize the fourth order ΣΔM developed in this work are treated in detail in chapter number five, where the system design of a three-mode ΣΔM is presented.

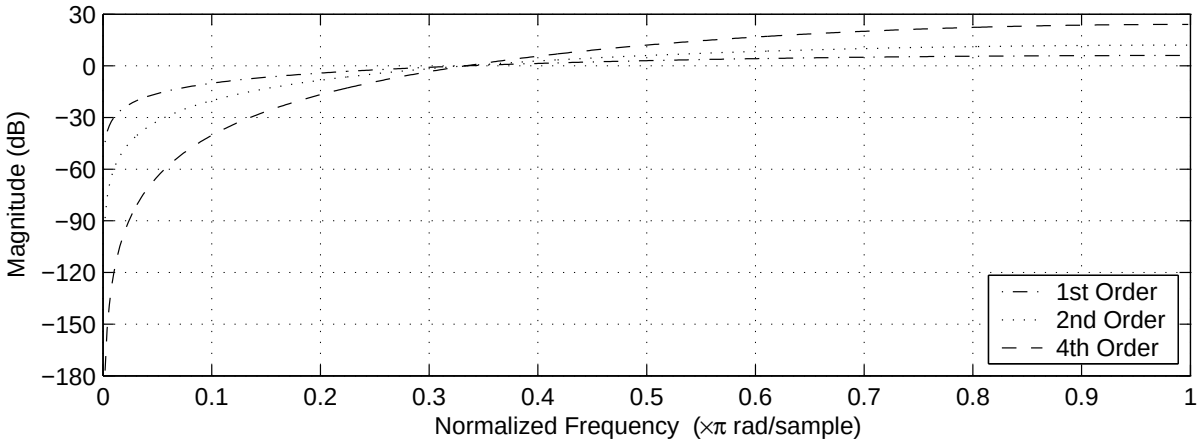

Figure 3.14: Frequency response of 1st-, 2nd, and 4th- order noise differencing *NTF*'s.

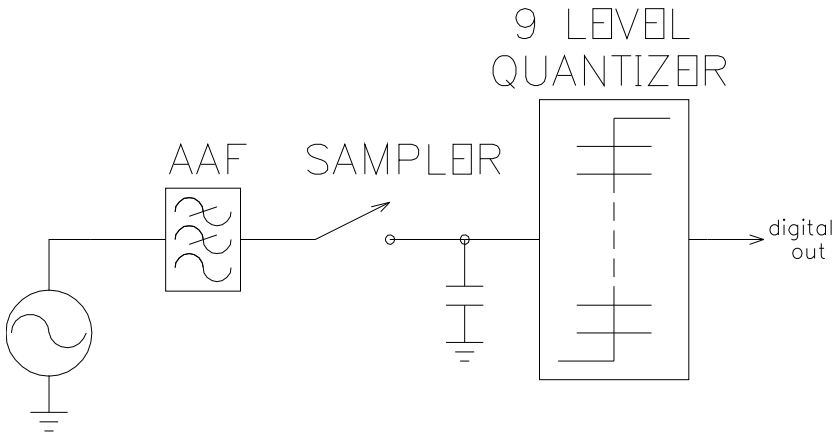

Figure 3.15: Oversampled analog-to-digital conversion used by Galton.

3.4.5 Spurious Performance of Sigma Delta Modulators

At this point, the following question can arrive:

"if ΣΔM's are prone to instability, why to use them for the digitization of signals in wireless receivers instead of uniform quantizers plus oversampling?"

The answer is found to be in the tonal behavior of ΣΔM's when compared with uniform quantizers that use oversampling. In wireless communications the SFDR perfomance of an ADC is very important because it is directly related with the ability of the ADC to separate a small incoming signal from ADC noise spikes. To clarify this situation the example proposed by Galton [14] is reproduced in this section. The experiment consists in its first part, of performing the *fast Fourier transform* (FFT) of an oversampled signal that has been converted to the digital domain by a nine-level uniform quantizer, as shown in figure 3.15.

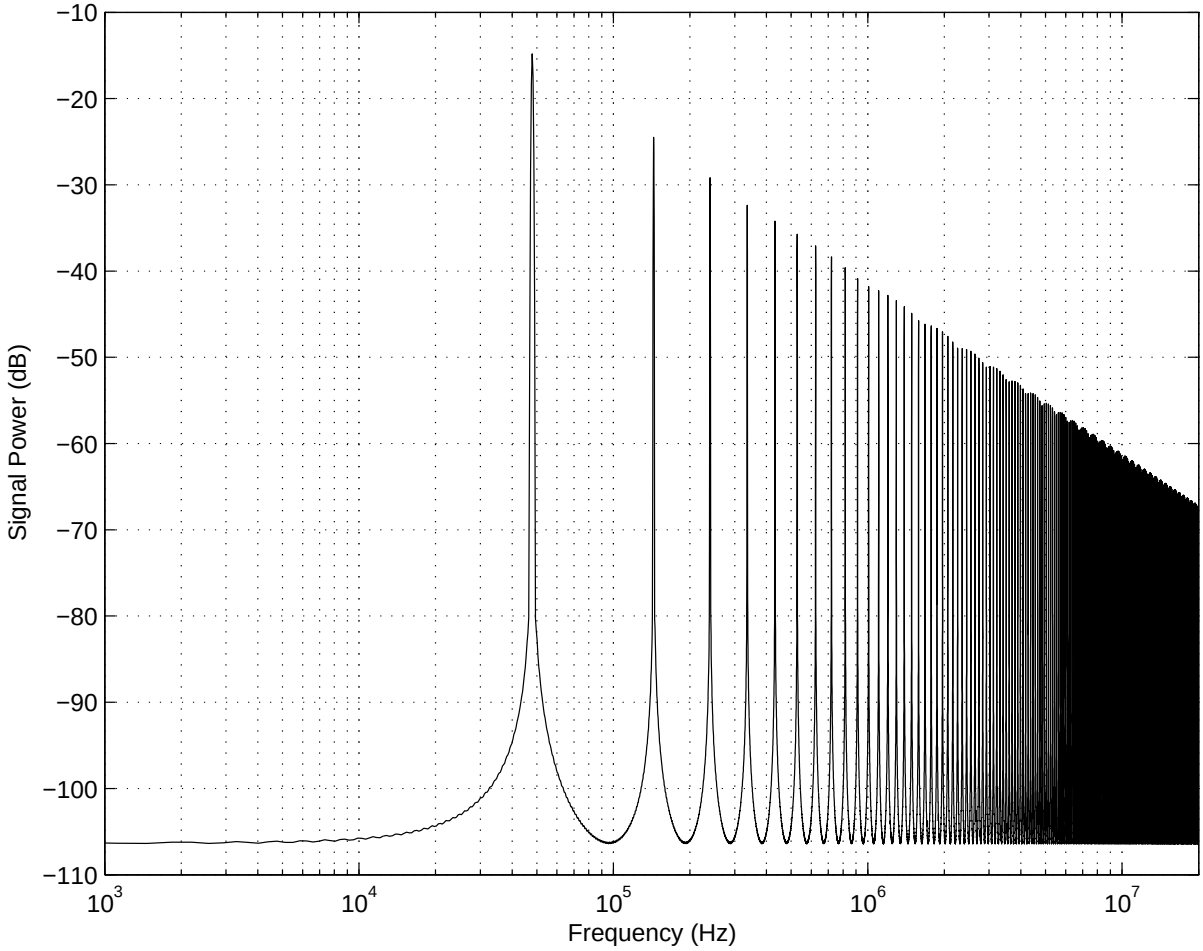

Figure 3.16: Spectrum of a 48kHz sinus digitized by a 9-level quantizer.

Here, a sinusoidal input with 48 kHz of frequency is sampled at 48 MHz and quantized by a 9-level uniform quantizer, the f_b extends from 0 to 500 kHz resulting in an $OSR = 48$. This array was simulated in *MIDAS* [31] and the FFT of the digital output was obtained. The resulting spectrum is depicted in figure 3.16, from that, a very poor SFDR, which is the difference between the input signal and the largest in-band harmonic, of only 10dB is observed. In the band from 0 to 500 kHz the SNR is only 14 dB.

Next, the same quantizer is embedded in a second order ΣΔM. The resulting system can be seen in figure number 3.17. In this case the input signal stills being sampled at the same rate. This modulator was modeled and simulated with the same program as the first system. The FFT of the output was also performed, taking care of simulating the same quantity of input cycles. The resulting spectrum of the obtained output is presented in figure 3.18

Unlike the nine-level quantizer alone, the ΣΔM has well-behaved quantization noise because it is subjected to two DC zeroes, which brings as a consequence that its power resides mostly at

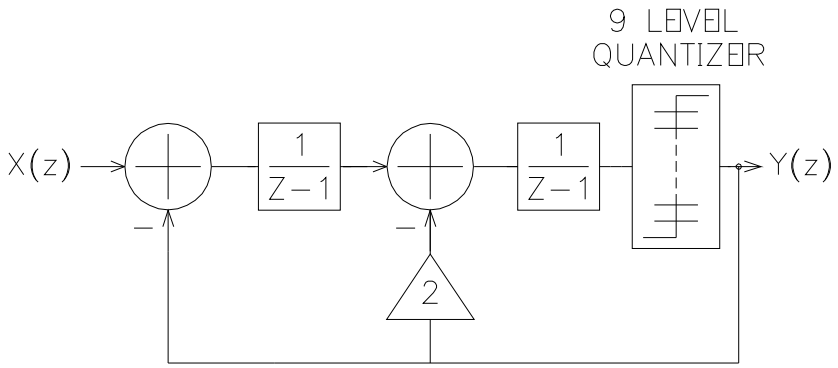

Figure 3.17: A 9-level quantizer embedded in a second order ΣΔM.

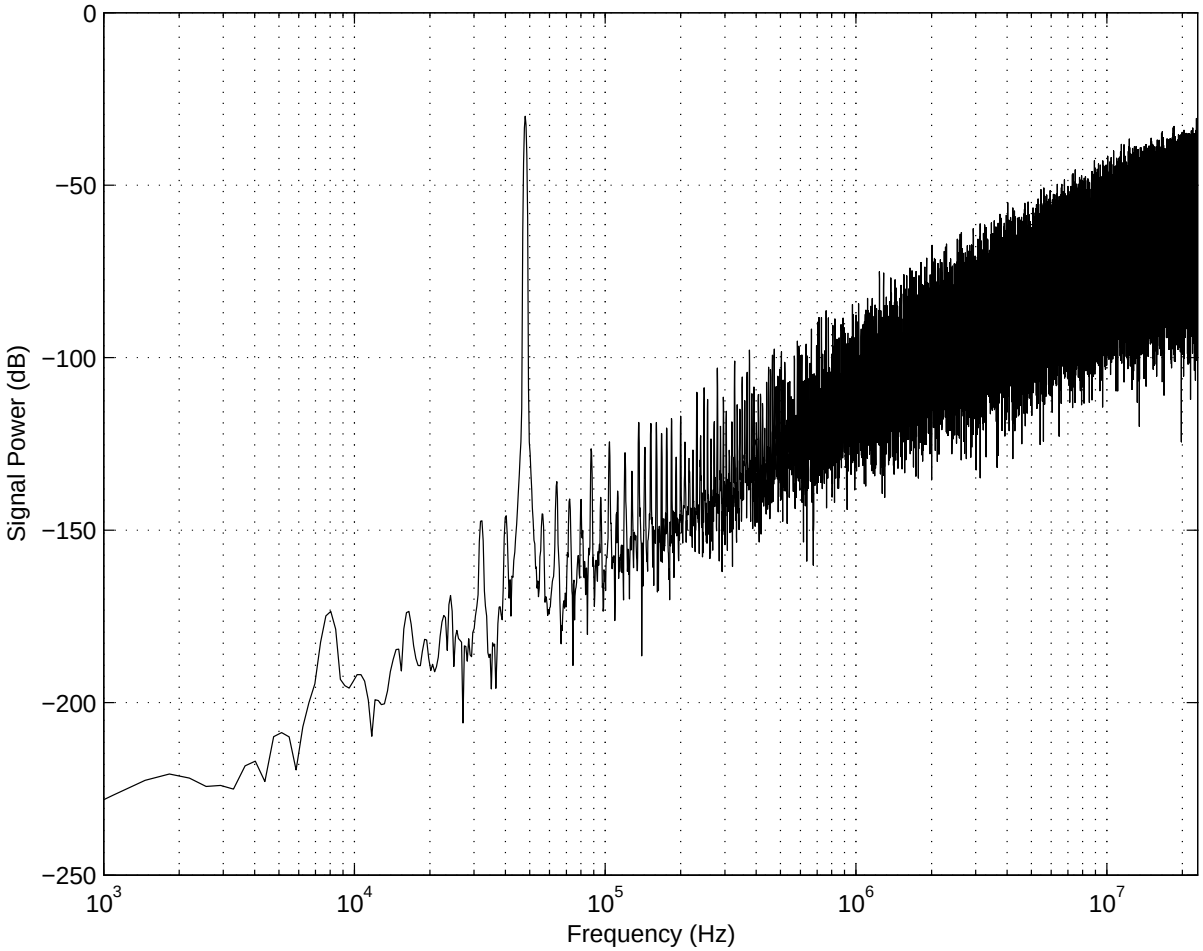

Figure 3.18: Spectrum of a 48kHz sinus digitized by a second order ΣΔM.

high frequencies. As it can be seen in the last graphic, in the band from 0 to 500 kHz, we do not have any spurious tones. Estimated from the power spectrum, in the band of interest, the SNR is equal to 84 dB.

This result clearly shows the high linearity of the ADC's based on ΣΔM's, which is reflected in a high SFDR. This is a very desirable characteristic in the wireless communications scenario because a very small signal must be detected in presence of much bigger interferers that lie near the desired frequency. Furthermore, as required by digital IF receivers, ΣΔM's can be designed to suppress the quantization noise in a certain band of interest centered a way from DC. This is accomplished by the so called *bandpass sigma-delta modulation* (BPΣΔ), which is discussed in the next section.

3.5 Bandpass Sigma Delta Modulation

As presented in the last section, the building blocks of a lowpass ΣΔM are integrators having an infinite voltage gain at DC. In fact, the poles of the integrators are the cause of the zeros in the NTF. From (3.11), if $A(z)$ is a function of the form:

$$A(z) = \frac{(zero_1 + z)(zero_2 + z)\cdots(zero_n + z)}{(pole_1 + z)(pole_2 + z)\cdots(pole_n + z)} \tag{3.25}$$

then the NTF takes the form:

$$NTF(z) = \frac{(pole_1 + z)(pole_2 + z)\cdots(pole_n + z)}{((pole_1 + z)(pole_2 + z)\cdots(pole_n + z)) + ((zero_1 + z)(zero_2 + z)\cdots(zero_n + z))} \tag{3.26}$$

As it can be seen, the *poles* of the function in the forward path of a noise shaping loop become the *zeros* of the NTF. This fact can be used to suppress the quantization noise at certain frequency located at any place between DC and $f_s/2$. This is accomplished if the integrators in the forward path of the already presented ΣΔM's are replaced with *resonators* having infinite gain at the frequency of interest. The most common way to design the resonators required in a bandpass sigma-delta modulator (BPΣΔM) is to take the integrators of an already designed lowpass modulator and to apply a *lowpass to bandpass transformation*. The most important frequency transformations are going to be presented in the next section.

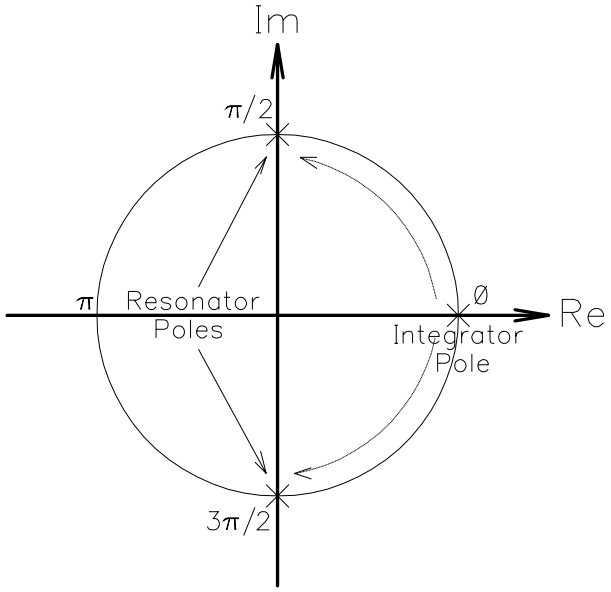

Figure 3.19: Effect of the transformation over the pole of an integrator.

3.5.1 Spectral Transformations for the High Level Design of Resonators

A general lowpass to bandpass transformation is the one proposed by Constantinides [32]:

$$z^{-1} \rightarrow \frac{-z^{-2} + \cos(2\pi f_c / f_s) z^{-1}}{1 - \cos(2\pi f_c / f_s) z^{-1}} \tag{3.27}$$

This transformation allows to put the poles of the resonators at any angle between 0 and π in a normalized discrete time frequency axis. For the particular case, in which the ratio of the resonant frequency (f_c) to f_s equals to $1/4$, (3.27) reduces to:

$$z^{-1} \rightarrow \frac{-z^{-2} + \cos(\pi/2) z^{-1}}{1 - \cos(\pi/2) z^{-1}}$$
$$z^{-1} \rightarrow -z^{-2} \tag{3.28}$$

(3.28) is a very popular transformation and has been applied many times by designing BPΣΔM's that suppress the quantization noise at $f_s/4$, this is a very desirable characteristic that a IF digitizer for radio receivers should posses, because this reduces the separation of the I and Q channels at the digital domain to a multiplication by a sinus and a cosinus running at $f_s/4$, which is equivalent to multiplication by 1, 0, -1, 0. Applying (3.28) to a discrete-time delayed integrator produces a resonator having the transfer function:

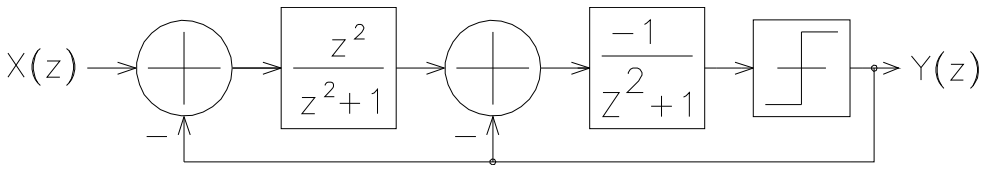

Figure 3.20: Architecture of a fourth order bandpass sigma-delta modulator.

$$H_{res}(z) = \frac{z^{-1}}{1-z^{-1}}\bigg\|_{z^{-1}=-z^{-2}} = \frac{-z^{-2}}{1+z^{-2}} \tag{3.29}$$

The effect of the transformation can be observed by finding out the poles of the resulting resonator. Equation (3.29) has two imaginary poles at $\pm j$. The transformation has produced a resonator with infinite gain at $\pi/2$ and $3\pi/2$ in a normalized discrete time frequency axis. As it can be seen on figure 3.19, the single pole at DC of the integrator, was split after the transformation in two.

Similarly, if this transformation is applied to the second order ΣΔM of figure 3.11, the BPΣΔM shown in figure 3.20 is obtained. Substituting the comparator by the linear model of figure 3.5, the output of this system, in the z-domain can be found to be:

$$Y(z) = \frac{-1}{z^2}X(z) + \frac{(z^2+1)^2}{z^2} = -z^{-2}X(z) + (1+z^{-2})^2E(z) \tag{3.30}$$

After (3.30) the NTF is found to be $(1+z^{-2})^2$. This function has two transmission zeros at $\pi/2$ and $3\pi/2$ and suppresses the quantization noise power spectral density N_e arround those frequencies. The in-band quantization noise power (P_e) can be calculated by making $z = \exp(2\pi j f/f_s)$ where f_s is the sampling frequency and after that, integrating the output power spectral density within the signal bandwidth (f_b), it is assumed that f_b is centered at $f_s/4$ (i.e. $\pi/2$):

$$P_e = \int_{f_s/4-f_b/2}^{f_s/4+f_b/2} \left|(1+z^{-2})^2\right|^2 N_e df = \int_{f_s/4-f_b/2}^{f_s/4+f_b/2} |(1+\exp(-4\pi j f_N))|^2 2\frac{\Delta^2}{12 f_s} f_s d f_N \tag{3.31}$$

In (3.31) the change of variable $f_N = f/f_s$ has been done, then $df = f_s d f_N$. Since $|a \pm jb|^2 = a^2 + b^2$, (3.31) can be rewritten as:

$$P_e = \int_{f_s/4-f_b/2}^{f_s/4+f_b/2} |(1+\exp(4\pi j f_N))|^2 2\frac{\Delta^2}{12 f_s} f_s d f_N \tag{3.32}$$

To evaluate the integral, the term $|(1+\exp(4\pi j f_N))|^2$ can be expanded using *Taylor Series* around $f_N = 1/4$ the first term of the series is $256\pi^4 f_N^4$, using this result to solve the integral it is obtained:

$$P_e \approx \frac{\Delta^2 \pi^4}{60 \times OSR^5} \tag{3.33}$$

From (3.33) and assuming that the modulator input is a sine wave of amplitude $A \leq \Delta/2$ the *SQNR* and *DR* are given by:

$$SQNR = \frac{A^2}{2P_e} = \frac{30 \times A^2 \times OSR^5}{\pi^4 \Delta^2} \tag{3.34}$$

$$DR = \frac{(\Delta/2)^2}{2P_e} = \frac{15 \times OSR^5}{2\pi^4} \tag{3.35}$$

This relationships show that the resolution and dynamic range of this fourth order BPΣΔM increase with *OSR* at a ratio of 2.5 bit per octave, as it is the case of a second order low pass ΣΔM, this is because it should be understood that there are only two zeros in the noise transfer function at $f_s/4$, with the other two zeros located at $-f_s/4$, and so, the quantization noise is only suppressed with a second-order bandstop transfer function in the signal passband. For lowpass modulators, there is no discrepancy between the order of the noise transfer function and the number of zeros that suppress the quantization noise around DC; they are equivalent. But, for bandpass modulators, the order of the modulator strictly refers to the number of zeros in $NTF(z)$.

The modulator under analysis was modeled and simulated with *MIDAS* using a $f_s = 168$MHz and a sinusoidal input signal of frequency equal to 42MHz. The spectrum of the output of this modulator was obtained as well; the result is shown in figure 3.21. As it can be seen the quantization noise is effectively suppressed in a region closer to $f_s/4$.

The *SQNR* was obtained for different input levels and estimated from the output spectrum. For an *OSR* of 61, the results are shown in figure 3.22. Comparing the peak *SQNR* obtained from simulation, a very close value to the one predicted by equation 3.34 is observed, which is equal to 84dB if $\Delta = 1$. This result shows the validity of the assumptions taken over the nature of the quantization noise, as well as that of the method used to calculate the quantization noise power (P_e) and presented in [33].

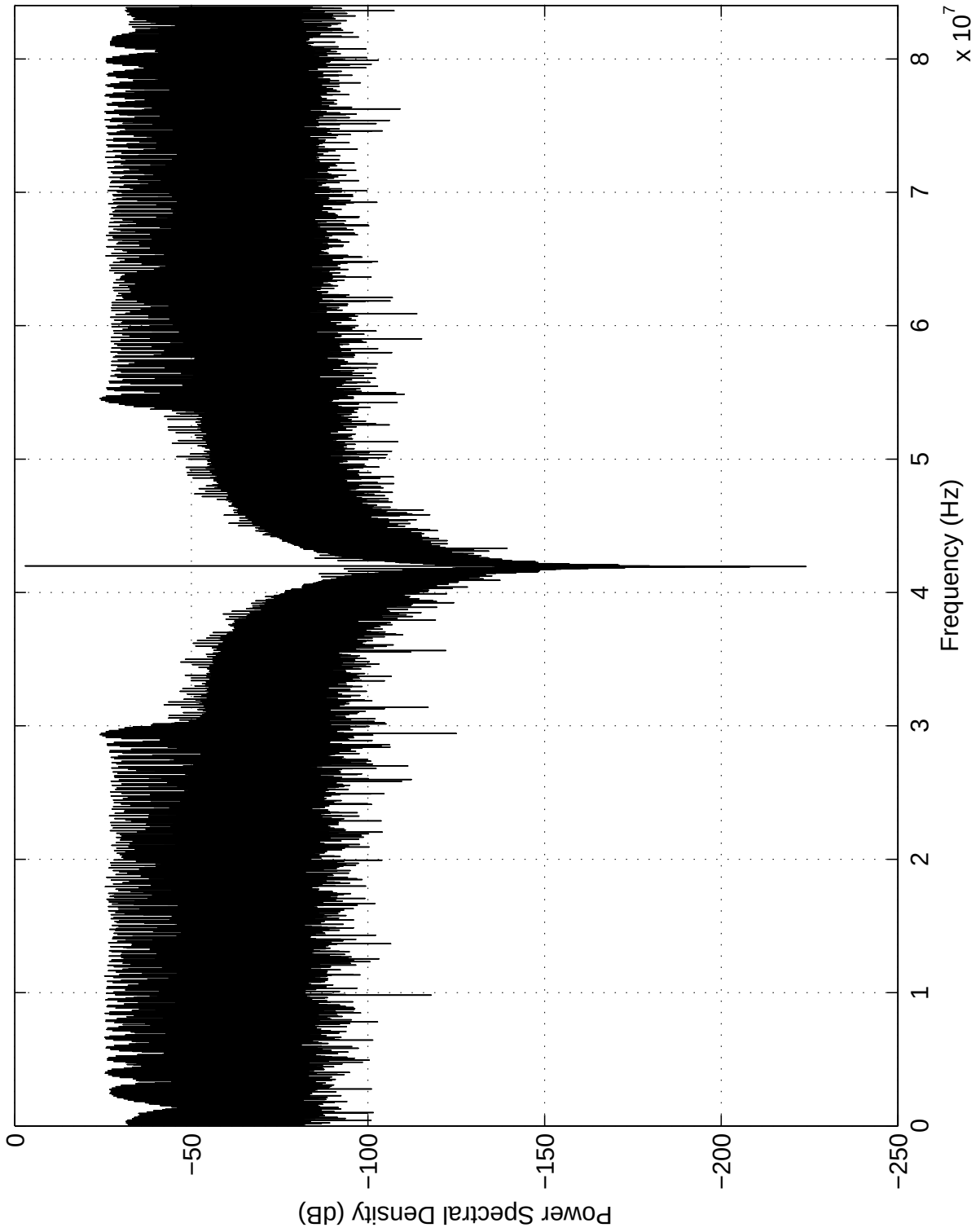

Figure 3.21: Spectrum of the output signal of a fourth order bandpass sigma-delta modulator.

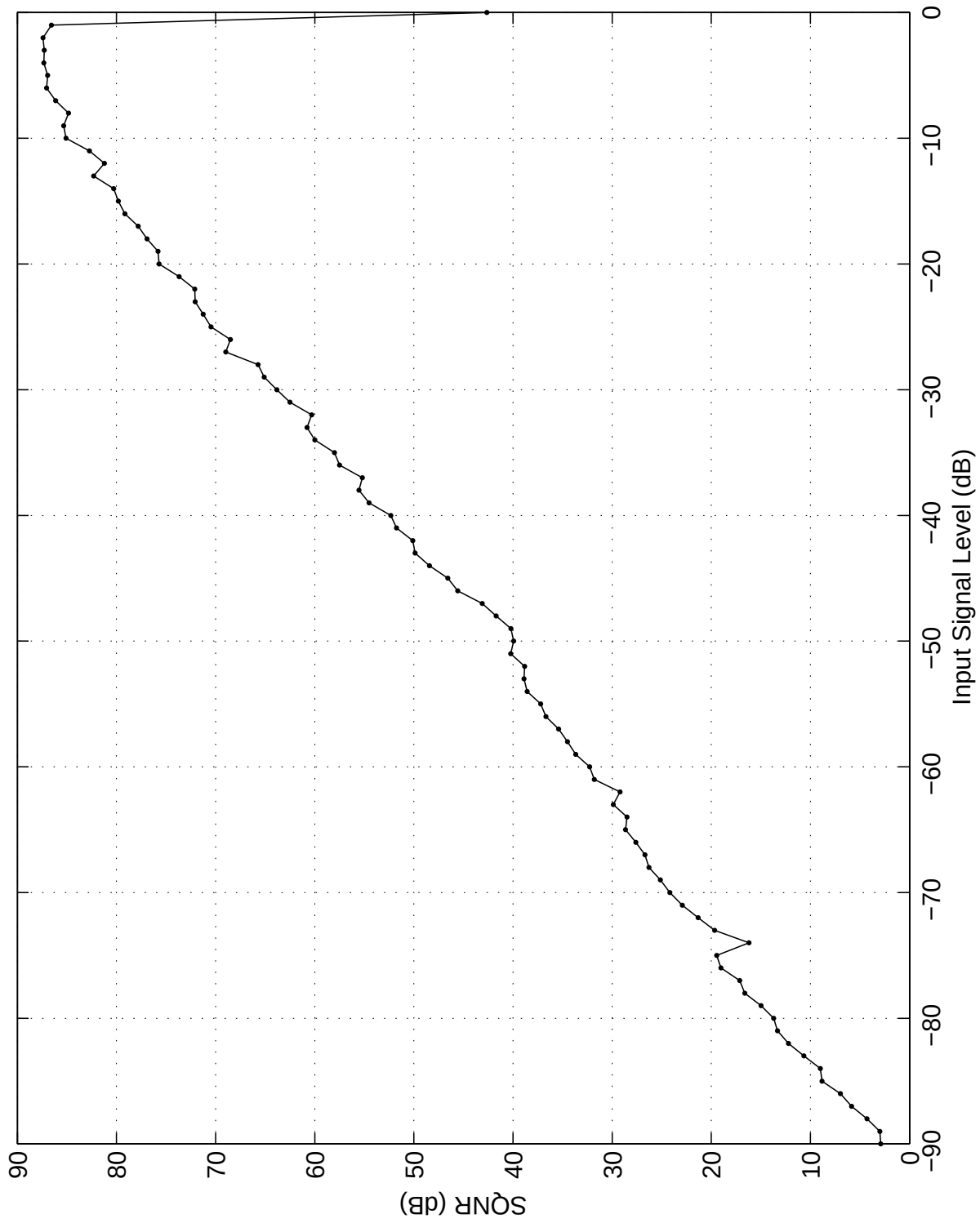

Figure 3.22: SQNR vs. input signal level of a fourth order bandpass sigma-delta modulator.

Another family of resonators is obtained using the continuous to discrete time *Bilinear Transformation*. Here a continuous time resonator at ω_C is transformed into a discrete time IIR filter with central frequency ω_D by performing the operation [23]:

$$H_D(z) = H_C(s)\Big|_{s=\frac{1-z^{-1}}{1+z^{-1}}} \tag{3.36}$$

The correspondence between the frequencies is obtained using the non-linear mapping:

$$\omega_D = 2\arctan(\omega_C) \tag{3.37}$$

Now, the integrators of the second order lowpass ΣΔM depcited in the figure 3.11 are going to be replaced with resonators designed using (3.36), which were derived form continuous time resonators having the transfer function:

$$H_C(s) = \frac{1}{s^2 + {\omega_C}^2} \tag{3.38}$$

Using (3.37) with $\omega_D = \pi/2$ it is obtained:

$$H(s) = \frac{1}{s^2 + 1} \tag{3.39}$$

Applying the bilinear transformation over the last equation it is produced:

$$H(z) = \frac{1}{2} + \frac{z^{-1}}{1+z^{-2}} \tag{3.40}$$

A delay free branch not realizable in switched capacitor is present. Multiplying the last equation by $-z^{-1}$ adds the needed delay:

$$H(z) = -\frac{1}{2}z^{-1} - \frac{z^{-2}}{1+z^{-2}} \tag{3.41}$$

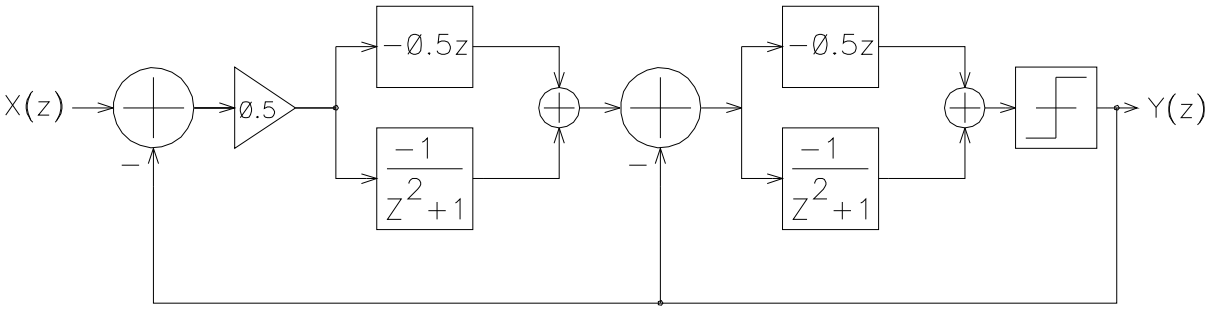

Figure 3.23: A fourth order bandpass sigma-delta modulator whose resonators were derived from continuous time prototypes.

The resulting architecture is shown in the figure 3.23.

For the BPΣΔM of figure 3.23 the linearized analysis produces the following expressions for the STF and NTF respectively:

$$STF(z) = \frac{1+4z+6z^2+4z^3+z^4}{1+6z^2-4z^3+9z^4-4z^5+8z^6} \tag{3.42}$$

$$NTF(z) = \frac{8z^2+16z^4+8z^6}{1+6z^2-4z^3+9z^4-4z^5+8z^6} \tag{3.43}$$

The quantization noise power spectral density N_e is shaped by eq. (3.43), which has zeros at $(0,\pi/2,3\pi/2)$. Proceeding in the same way as for the architecture in figure 3.20, after the substitution of z by $\exp(2\pi j f/f_s)$, the first term of the Taylor series is $1024\pi^4/{f_N}^4$ and the approximated value of P_e is given in eq. (3.44). Using this result, expressions for the *SQNR* and *DR* are found in (3.45) and (3.46). The linear analysis of this architecture shows that the resolution and *DR* also increase 2.5 bit per octave of *OSR*, but comparing them with equations (3.34) and (3.35) it can be found that, for a given *OSR* the BPΣΔM depicted in figure 3.23 will reach one bit less of resolution than the BPΣΔM shown in figure 3.20.

$$P_e = \frac{\Delta^2\pi^4}{15\times OSR^5} \tag{3.44}$$

$$SQNR = \frac{15\times A^2\times OSR^5}{2\Delta^2\pi^4} \tag{3.45}$$

$$DR = \frac{15 \times OSR^5}{8\pi^4} \tag{3.46}$$

In order to prove these results, modeling and simulation of this BPΣΔM was conducted in the same way, as for the former case. The spectrum of the output signal can be seen in figure 3.24. The sampling frequency and the *OSR* used in the simulations were also 168MHz and 61. Results of the estimated *SQNR* are also closed to the values given by equation 3.45. This characteristic curve is presented in figure 3.25.

3.6 Summary

In this chapter the fundamental theory behind the analog-to-digital conversion process was addressed. The conducted analysis presented the characteristics of the Nyquist-Rate converters as well as the advantages that can be reached by usign such converters plus oversampling. This section also treated in detail how the quantization noise coming from the conversion procedure can be filtered at base band or around certain frequency by means of the sigma-delta modulation. This conversion method was analyzed both in the lowpass and in the bandpass case, comparisons realized between this method and a Nyquist-Rate converter, show how the sigma-delta modulation posses a much better performance concerning the SFDR characteristic of an ADC, being this fact the cause why these ADC's are the ones dominating the wireless communications arena. Of special interest for the development of wireless receivers with digitization at IF, is the bandpass sigma-delta modulation, for this class of sigma-delta modulators, the most important spectral transformations for the high level design of the required resonators were presented without taking care of circuit implementation details. As it will be analyzed in the chapter number five, the circuit implementation of such resonators can be carried out at least in two different ways, having significant effect on the required characteristics of the circuit elements needed for their implementation. The analysis presented in that chapter justifies the chosen implementation of such resonators in the experimental prototype developed during this work. It can be also mentioned, that as the most often used transformation, $z^{-1} \rightarrow z^{-2}$ produces a sigma-delta modulator, which suppresses the quantization noise in a region near to $f_s/4$, digitizing an IF signal centered at f_{IF} asks for $f_s = 4 \times f_{IF}$ having in mind practical values of the IF used in mobile phone systems, has lead this transformation to sampling rates so high, that, up to the point of writing this work, the developed IF digitizers designed using this transformation can not fulfill the low-power constraints of battery-powered mobile communications equipment. Of course, the attractive idea of converting an IF signal to the digital domain, as described in the preceding chapter, has brought extensive research work directed to the low-power consumption implementation of BPΣΔM's at $f_s/4$.

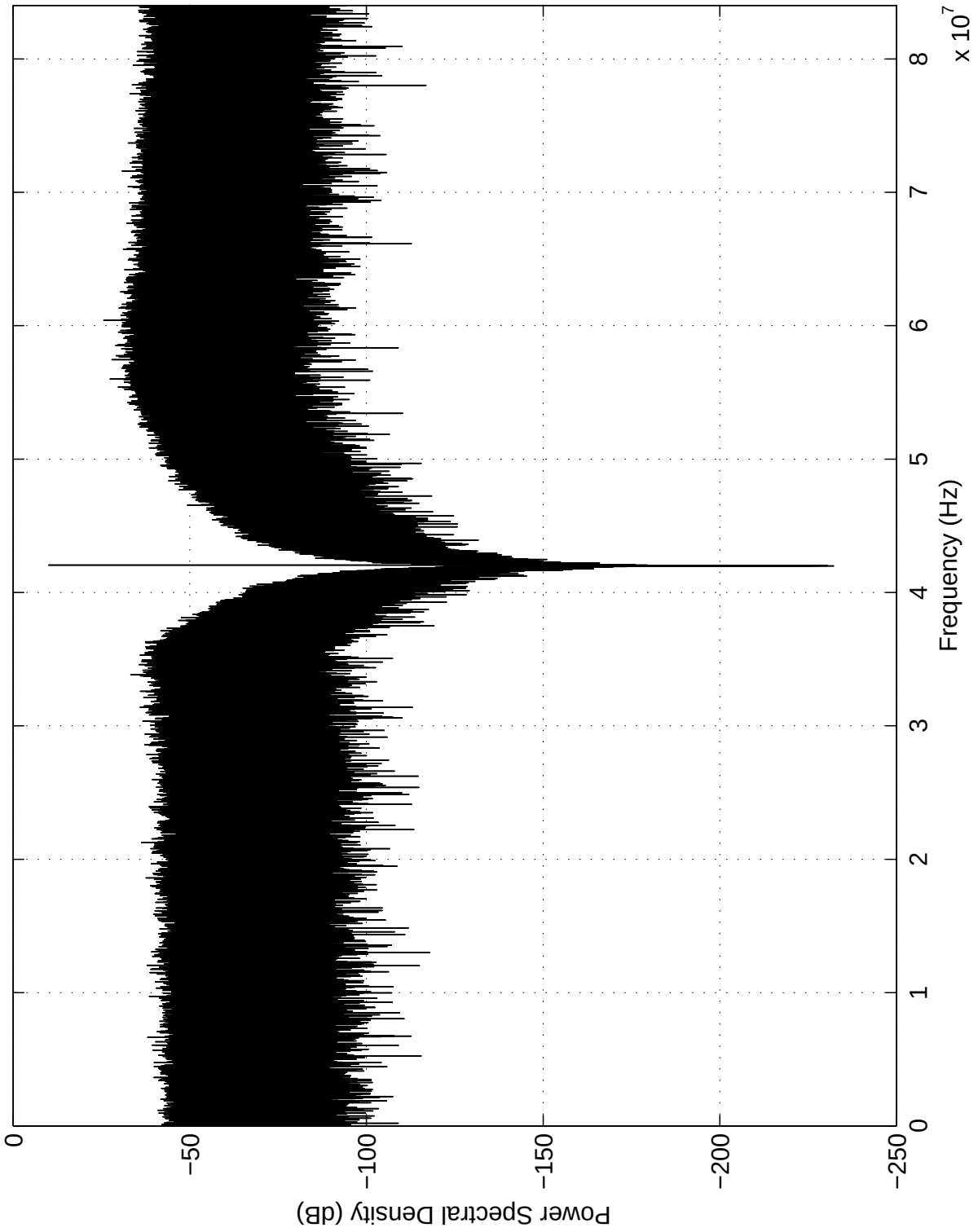

Figure 3.24: Output signal spectrum of the bandpass sigma-delta modulator of figure 3.23.

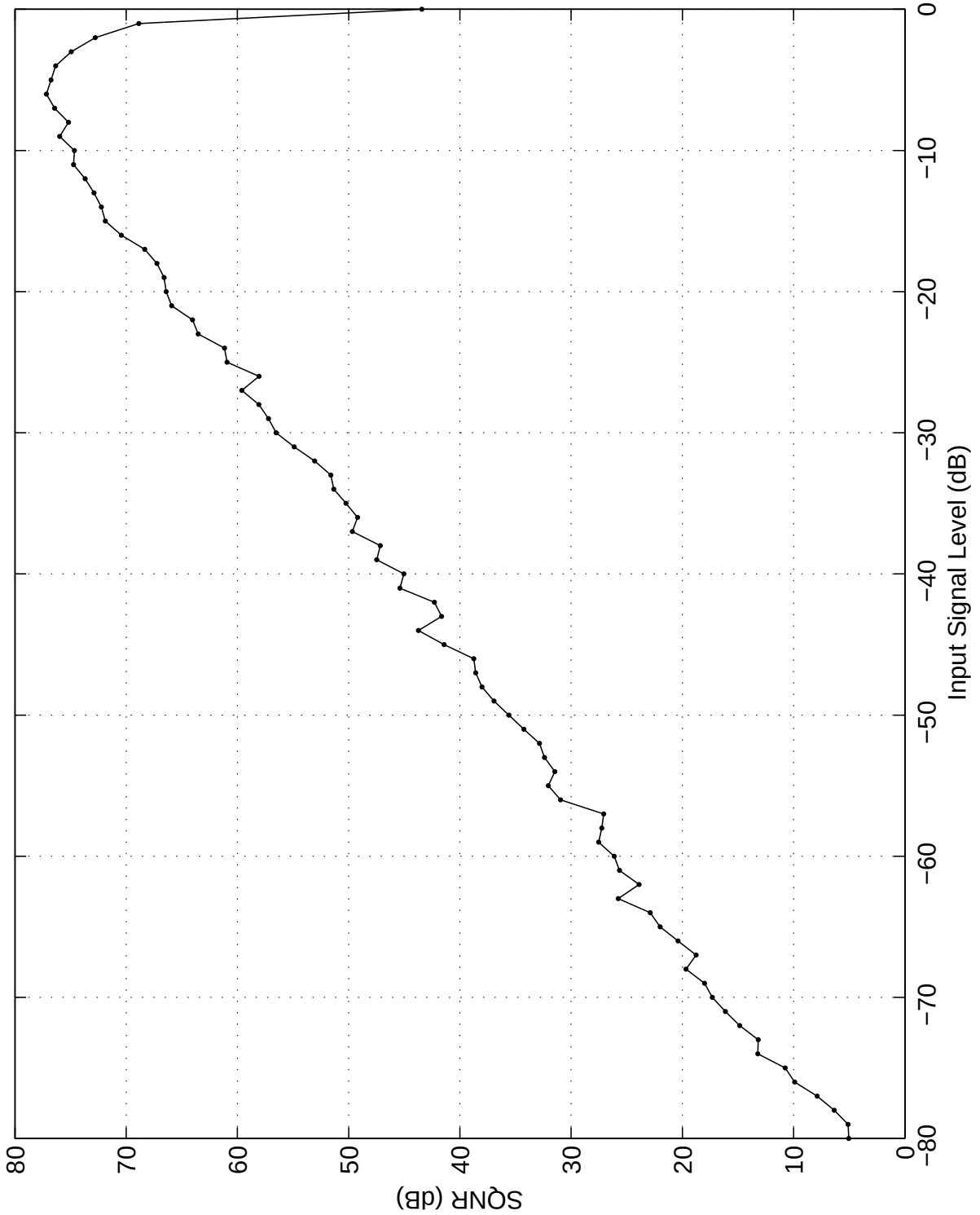

Figure 3.25: Simulated *SQNR* performance of the bandpass sigma-delta modulator of figure 3.23.

The next chapter deals with the up to date proposed methods, together with the proposed approach for the realization of dual standard mobile phones and contrasts those receiver architectures with respect to their flexibility, hardware reuse and, most important for this work, the characteristics imposed to the ADC's used in each approach.

Chapter 4

Approaches for Dual Standard Receivers

Contents

4.1 Introduction

This chapter presents the, to date, reported methods to realize mobile phones capable of managing signals with 2G/3G communication standard characteristics. As stated in chapter one, the transition between the second and third generation of mobile communications services can be significantly simplified by the design of reconfigurable mobile phones. This necessity is presented because even in the future, it is not expected that all suburban and rural areas are going to be covered by the new 3G services. Thus, 2G systems are also going to be present, demanding receivers capable of handling both 2G and 3G standards.

The architectures for dual standard mobile phones (DSMP) analyzed in this chapter share the hardware resources at the purely analog radio frequency (RF) front end and at the digital signal processing (DSP) in different ways. These architectures are aimed to manage the GSM and the UMTS systems, and they have been ordered in a chronological way, enabling the evolution of the approaches to be observed. Starting with the first method proposed by Burger in [3] the

reader can find the ideas of circuit and system designers used to tackle the challenging multi-standard reception problem in mobile telephony. The discussion finalizes with an original work presented in [12], which seems to achieve a good compromise between degree of integration and resource sharing, as well as in the derived dynamic range and speed requirements demanded from the ADC.

Due to the reasons exposed in the preceding chapter, the interface between the RF front end and the DSP has - in all these approaches - been done using ΣΔM's with programmable characteristics. Since these interfaces are of great interest for the present work, they were analyzed and simulated, where it was possible. Finally, the requirements on the ADC needed in the proposed solution are derived and some conclusions are given.

4.2 The Double Intermediate Frequency Architecture

One of the first approaches reported for the architecture of a DSMP was presented in [3]. In that work, the receiver had two separate RF paths as well as two different intermediate frequencies used for each standard. As it can be seen in figure 4.1, the reception method adopted in this design was based in the single-IF superheterodyne (SSH) architecture, a common structure for GSM receivers [34].

Dual mode operation was achieved by selecting each RF front end and reconfiguring the ΣΔM's at the IF-to-BB conversion stage in order to obtain the resolution imposed by each mode of operation. The characteristics of the components conforming the RF front-end were such that the required *DR* that should be exhibited by the ADC was approximately 88dB for GSM and 54dB for UMTS. The sampling rate chosen was determined as a multiple of the channel symbol rate of each system to facilitate decimation and detection in the digital receiver. The IF frequency (f_{IF}) was also linked with the sampling rate (f_s) in order to enable easy quadrature decomposition, so the IF frequency was placed at $4f_s/3$ instead of the more common $f_s/4$ to avoid excessive sampling rate for the ADC and the associated higher power consumption. Since the channel symbol rate is equal to 270.83 ksample/s and 3.84 Msample/s for GSM and UMTS respectively, the resulting effective sampling rates and *OSR* are 184.32 Msample/s with $OSR = 24$ for UMTS and 104 Msample/s with $OSR = 192$ for GSM.

The second frequency translation adopted in this receiver was the two-path IF sampling and mixing topology, as shown in Fig. 4.1, which has also been used in [35] and [36]. Here, the decomposition into *I* and *Q* branches is performed by sampling the input signal alternately for each branch at half the nominal sampling rate. The sampling instants between the two branches are offset by one sample period. The sampled signal is then mixed down to baseband by a

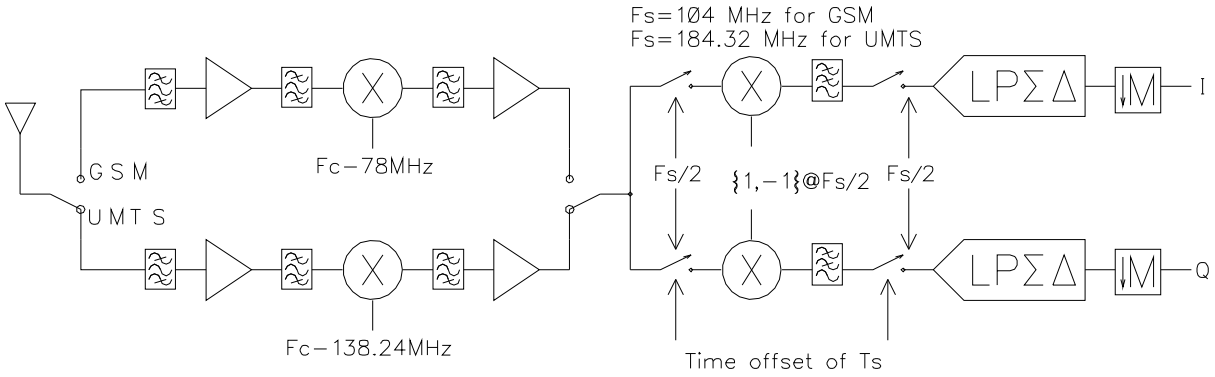

Figure 4.1: Architecture of a dual standard receiver proposed by Burger.

sequence of alternating +1's and -1's before being converted to digital representation by a low-pass modulator. This topology is mathematically equivalent to the more common method described in the last chapter in section 3.5.1, where a bandpass modulator is followed by a digital mixer, if the transform $z \rightarrow -z^{-2}$ is used for low-to-bandpass conversion, and the relationship $f_{IF} = (n - 1/4) f_s$ is valid between IF and sample rate.

The reconfigurability of the ΣΔM is shown at the architectural level in figure 4.2. A third order LPΣΔM was clocked at the already mentioned frequencies to obtain a signal to noise ratio (SNR) of 76 dB for GSM and 53 dB for UMTS. The cascade of integrators with feedforward was used with a zero at the border of the bandwidth for UMTS signals. This coefficient was inactive for GSM.

This architecture was modeled and simulated with *MIDAS* the output signal spectrum is shown in figure 4.3. Although the reconfigurability at the ΣΔM is achieved easily, a lack of resource sharing in the analog RF frontend of this receiver is observed making its integration a non-optimal task. Being the architecture in use the SSH, the usage of the passive filters for band and channel selection makes it also expensive to manufacture.

4.3 The Single Intermediate Frequency Architecture

To cope with the hardware resource sharing problem at the RF front-end, Salo et. al. [4] proposed the DSMP depicted in the figure 4.4. The approach used more shared building blocks in the RF front-end. Separate preselection and image rejection filters were required. A dual mode low noise amplifier (LNA) and a dual mode mixer were used [37]. A passive filter plays the role of anti-alias filter and channel selection filter for GSM and UMTS respectively. The GSM channel selection is performed digitally after the A/D conversion. The usage of dual mode LNA and mixer enabled operation at a single IF in both cases.

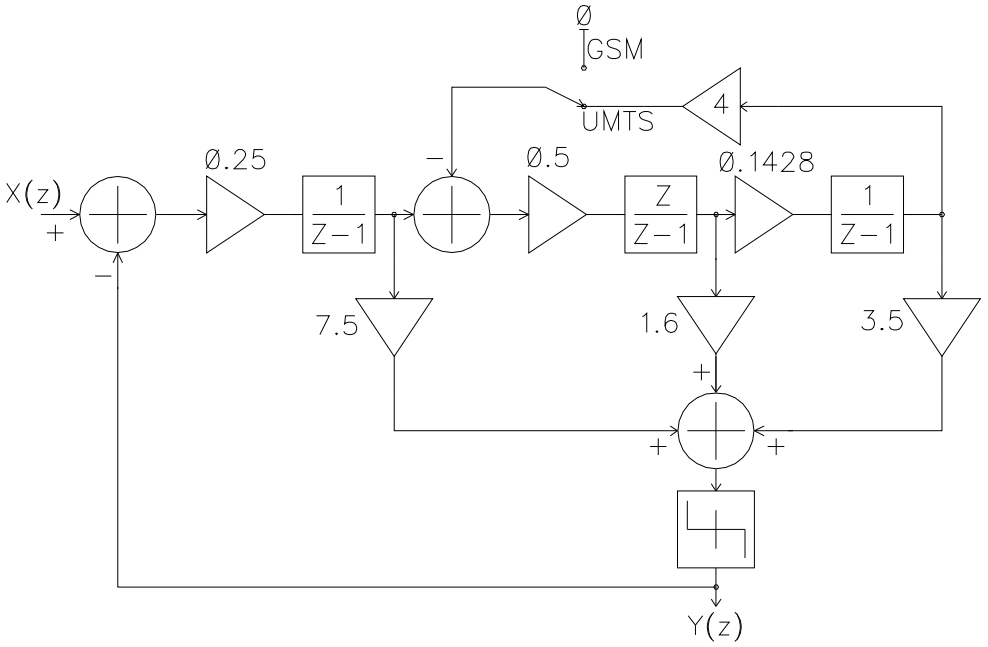

Figure 4.2: The reconfigurable lowpass ΣΔM used by Burger.

After the IF filter, the signal has to be amplified with variable gain before the A/D conversion. The IF signal is downconverted by subsampling to a second IF. A reconfigurable BPΣΔM was used for IF digitization. The architecture of that BPΣΔM is drawn in figure 4.5. The output signal from the ADC is digitally demodulated from the second IF, and the channel selections are performed/finalized in the digital domain. The analog I/Q demodulator and baseband filters are eliminated. The subsampling ratio between f_{IF} and the f_s was chosen according to $f_{IF} = (5/4)f_s$ producing a $f_s = 80$MHz.

Since the sampling frequency used was chosen to be a multiple of the UMTS chip rate, fractional decimation and interpolation are required in the GSM mode, however this non-integer relationship between f_s and channel rate for the GSM signals can lead to further complications not present when digital signal processing in the receiver is performed at channel symbol rate. In such a case the relative symbol clock frequency error between the transmitter and the receiver is only a few pulses per minute. This makes timing offset a slowly varying quantity that can be assumed constant over the duration of one block of symbols usually taken for efficient digital signal processing. Interpolation between samples to compensate for the timing offset then uses one set of filter coefficients per block of data. In contrast, when sample and symbol rate have a noninteger ratio, as in this present receiver, the timing offset varies from symbol to symbol, so that a different set of filter coefficients is needed for every different timing offset [38]. Therefore, the hardware implementation for noninteger sample-to-symbol rate conversion leads to substantial increase in chip area and/or power consumption. In the UMTS mode, a 4 bit ADC together with a DSP was implemented to improve SNR which is degraded due to the

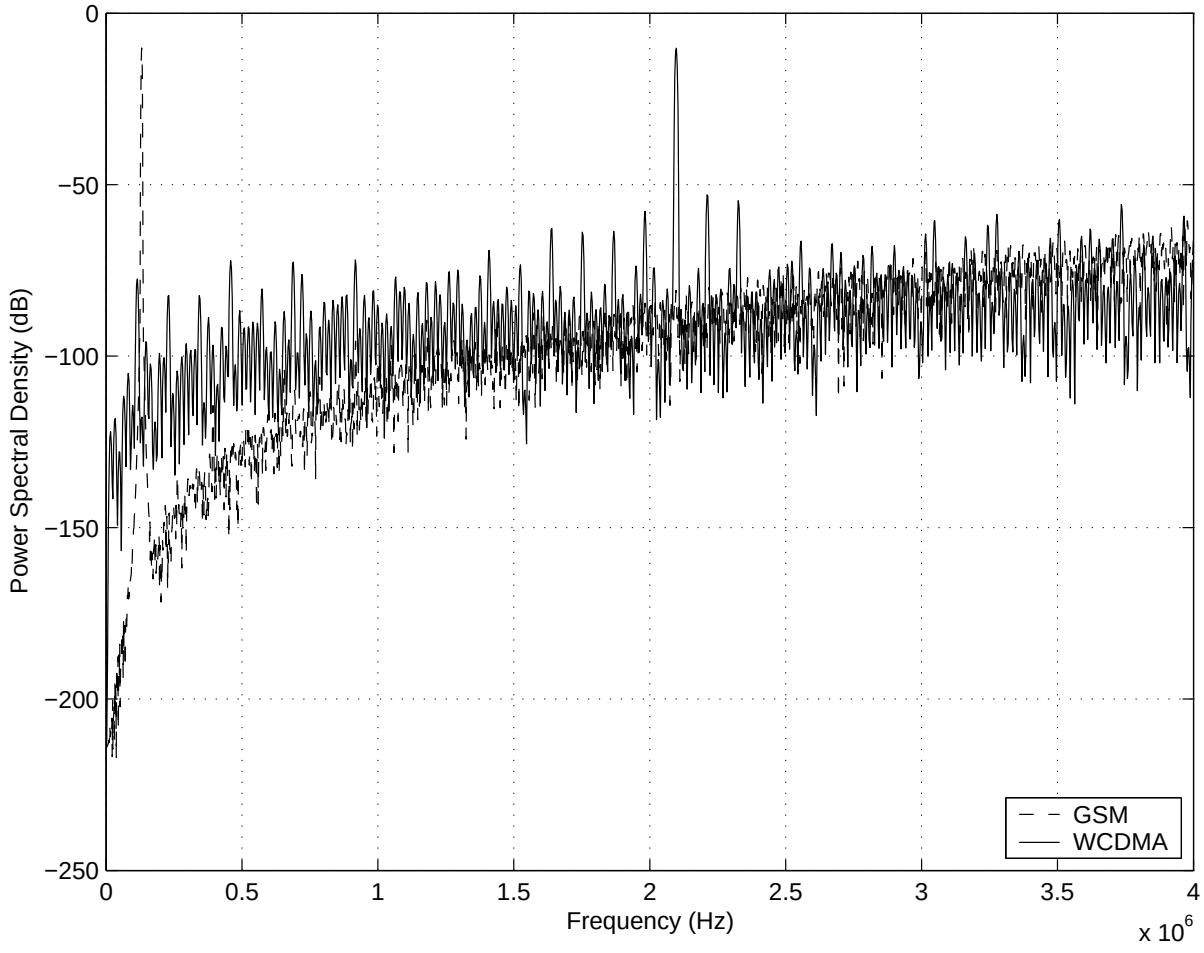

Figure 4.3: Output signal spectrum of the dual mode ΣΔM of fig. 4.2.

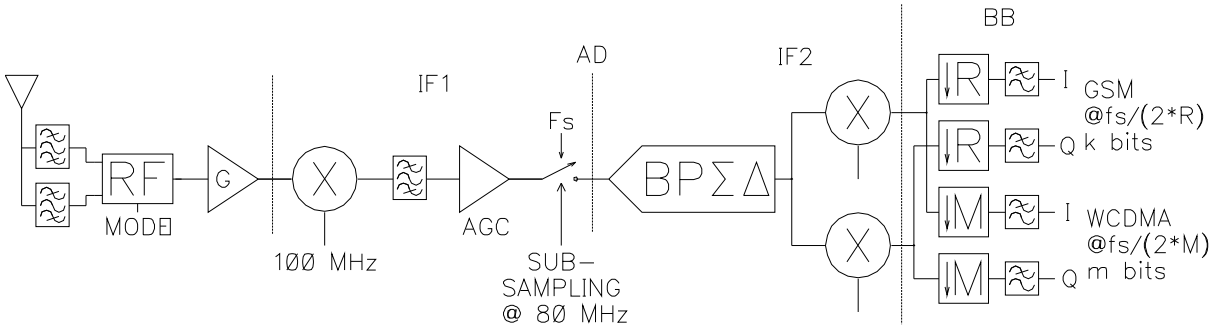

Figure 4.4: Architecture of a single IF DSMP

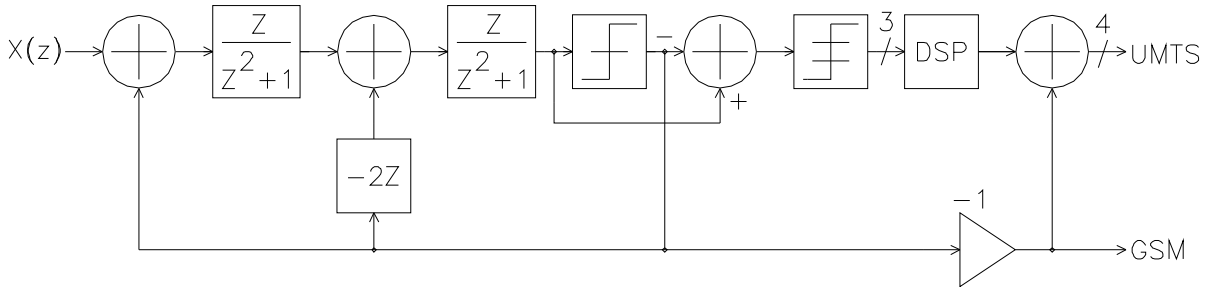

Figure 4.5: Dualmode bandpass sigma-delta modulator

fact that a lower oversampling ratio was used while keeping the same noise shaping as in the GSM mode. Peak SNR values of 78 dB and 48 dB were obtained for the GSM and the UMTS standards respectively. This dual mode ΣΔM was simulated in *MIDAS*. The spectrum of the output signal of this modulator is presented in figure 4.6

In addition to the already mentioned potential problems coming from the non integer *OSR* in the GSM mode, the 4 bit ADC plus DSP used in UMTS operation make the digital part of this receiver complicated, as does the SNR of 48dB reached in UMTS operation.This requires high selectivity blocks in the RF front-end, which are difficult to design.

4.4 The Zero IF - Low IF merged Architecture

The DSMP architecture proposed in [5] merges a zero-IF receiver for the UMTS standard and a low IF receiver for GSM into one system. As shown in chapter 2, the Zero-IF architecture offers the important advantage of being able to be integrated onto an IC without the need of expensive, off-chip IF filters. The known problems of this architecture concerning DC offsets and 2nd-order intermodulation products are not critical when the system is being operated within the wide band of UMTS signals and were solved by using AC couplings to filter out the DC offsets and some of the other second order products without significantly degrading sensitivity if the cut-off of these highpass filters is lower than 100 kHz. After the AC coupling, a pair of first order prefilters with a lowpass cut-off frequency of about 9 MHz attenuate some of the largest blocking interferers at frequency offset greater than 15 MHz. Before the ADC's, two AGC's are used in order to reduce the ADC dynamic range requirements. In that paper, a novel variation of the IF signal processing was introduced for the GSM mode. The authors proposed to digitize only the I component of the IF signal centered at a half of the total bandwidth (BW/2). As the full BW is being digitized, it is possible to make the digitized signal once again complex in the digital domain by performing a Hilbert transformation. To compensate for the loss of image rejection, caused by the digitization of only the I component of the IF signal, the usage

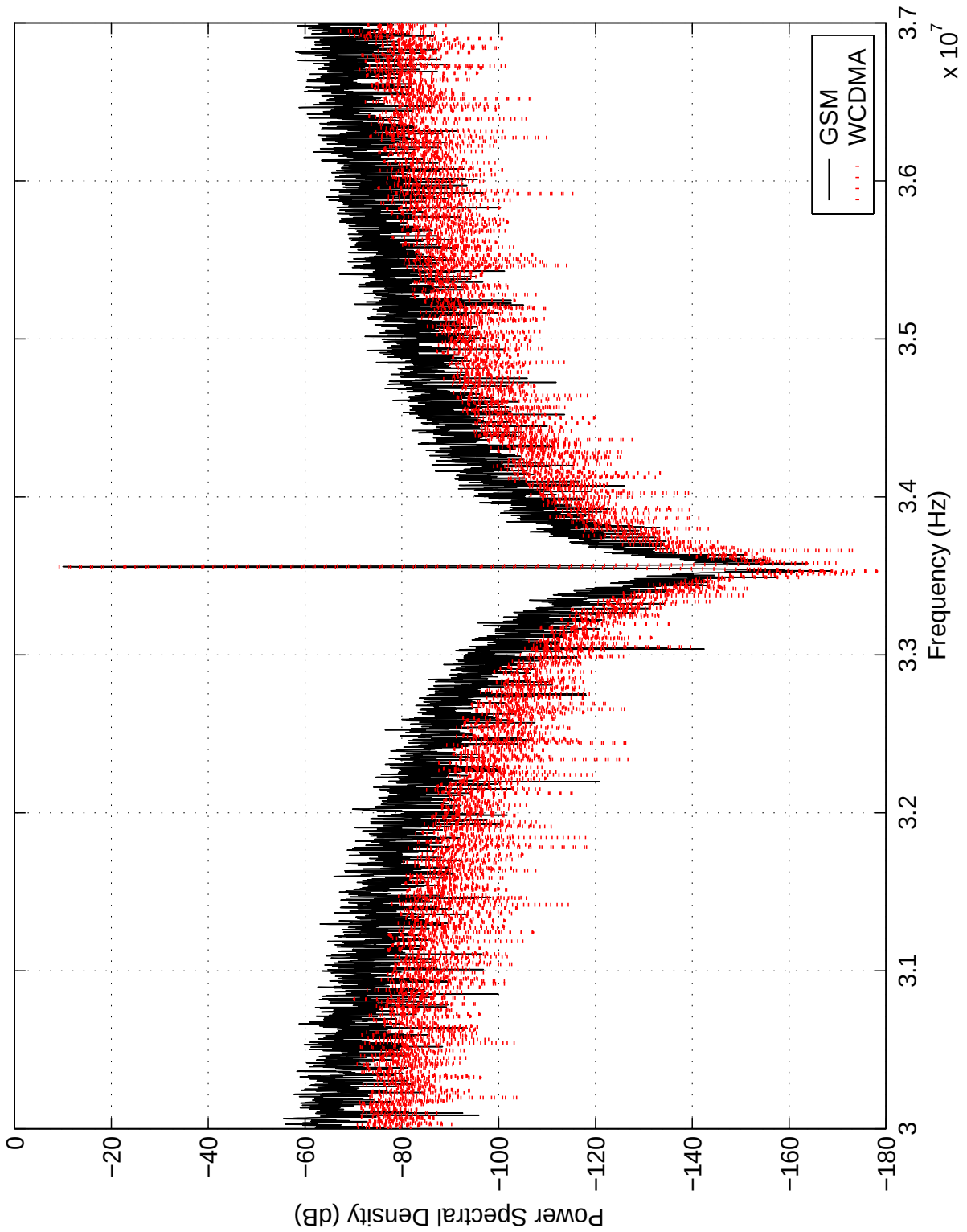

Figure 4.6: Output signal spectrum of a dual-mode BPΣΔM

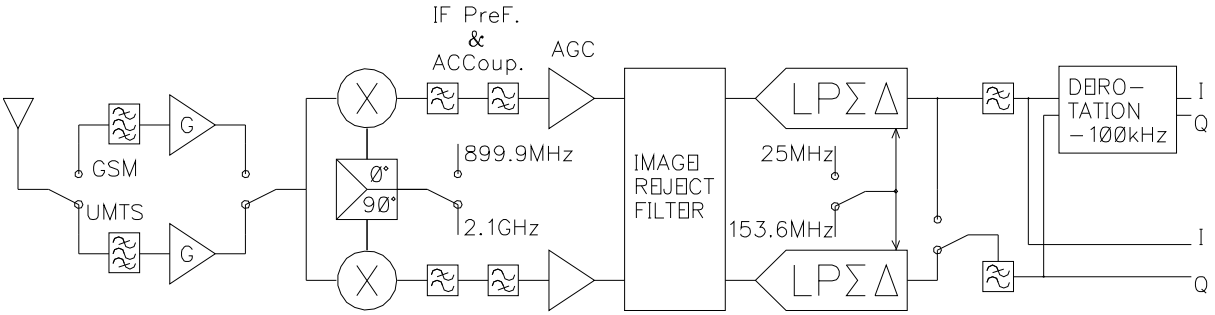

Figure 4.7: Architecture of a Zero IF - Low IF receiver

of a 3-stage passive polyphase filter (PPF) is necessary to provide an attenuation of about 30dB over the band -400kHz to zero. DC offsets coming from the mixers were removed by AC coupling whose highpass characteristics have a noncritical cut-off frequency around 10 kHz. This architecture is depicted in figure 4.7.

For both BB and low-IF digitization, fourth order continuous time LPΣΔM's with 1.5 bits quantization were used with clock rates of 25 MHz and 153.6 MHz producing an *OSR* of 48 and 20 for GSM and UMTS respectively. Because of the continuous time design of the here used ΣΔM's their modeling and simulation was not carried out. The interested reader can find detailed information about this circuit in [39]. When this receiver is operating in GSM mode, the whole RF *Q* path is not needed and one LPΣΔM is inactive, this conducts to a non optimal hardware resource sharing.

4.5 The proposed Approach

In the proposed solution an hybrid architecture was developed to achieve triple standard reception. The considered communication systems were: the second generation of personal communications according to the GSM standard, the third generation of wireless services UMTS and the short range ubiquitous connectivity standard *Bluetooth* (BT). This approach uses a low IF receiver for the GSM and BT standards and a Zero IF architecture for UMTS. Most of the constituent blocks at the RF front end can be reused, while at the IF-to-BB conversion a triple mode LPΣΔM is going to be used. In this architecture, only the band selection filters after the antenna as well as the image reject/channel select filters are separated for each standard. The careful selection of the IF in the GSM and BT sections of the receiver can reduce the image rejection requirements, so that passive poly-phase filters (PPF) can be employed. After channel filtering and image rejection, the signal has to be amplified with variable gain. This is accomplished by two AGC's placed before analog-to-digital conversion. The block diagram of this receiver is presented in figure 4.8.

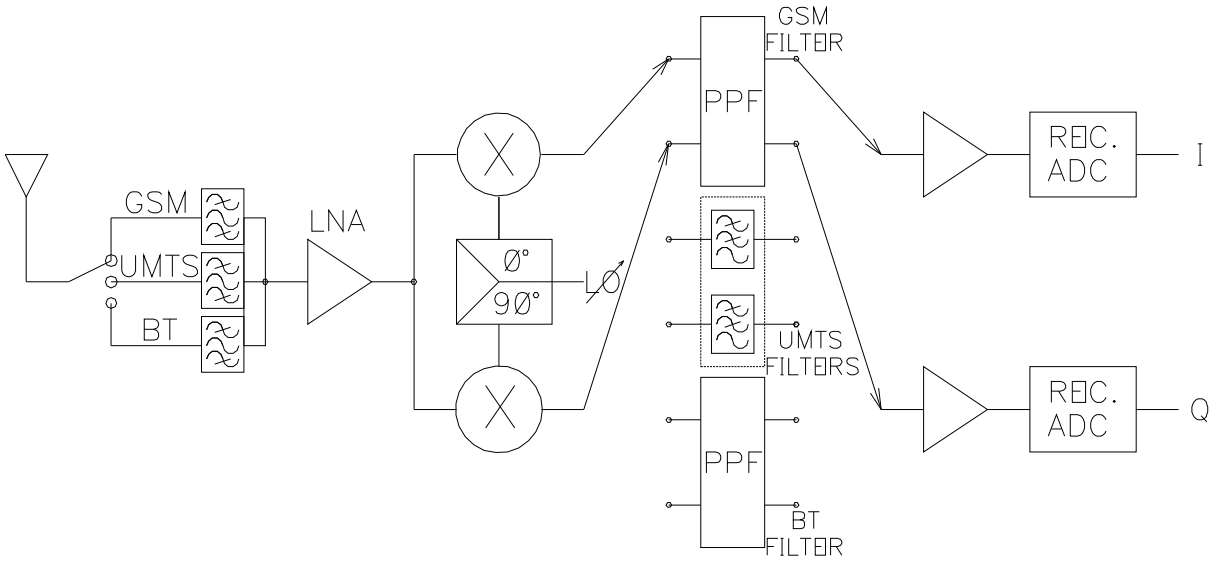

Figure 4.8: Architecture of the proposed multi-standard receiver

For the GSM standard, an intermediate frequency of 100 kHz is proposed. This value ensures that the image signal corresponds to the adjacent channel, which is only 9 dB higher than the wanted one and lies at an frequency offset of 200 kHz. At this frequency the required image rejection is of 22 dB. 400 kHz above the IF the alternate channel resides, which has a power 41 dB higher than that of the desired channel. This fact requires the tail of the alternate channel to be suppressed, requiring an image rejection of 35 dB.

The derivation of the design specifications for the constituent blocks of the RF front-end is an iterative process in which, the designer follows the input signals down the receiver chain to assign gain, dynamic range, linearity and noise figure to every block. The valid values of the components are those for which the receiver specifications are fulfilled. This task, known as *receiver planning*, is accomplished by RF engineers and is out of the scope of this work. The reader interested in the planning of the present receiver should consult [12] or, for a detailed version of the used method [13]. Our interest here concentrates on the derivation of the *SNR* imposed to the reconfigurable ΣΔM needed before DSP and whose analysis and design is one of the main subjects of this thesis. The *SNR* requirement is obtained after seeing the resulting power level profile of the desired signal plus interferers and blockers, as well as the noise floor presented at the input of the ADC. From this power level profile, the *SNR* is represented by the difference between the maximum signal level obtained at the output of the last block belonging to the RF front-end and the ADC input noise. In order to take into account the non-idealities presented in the implementation of the ADC, a 6dB margin is usually added to the value produced by the mentioned difference. A graphic showing the obtained power levels after the RF front end is depicted in figure 4.9. In the same figure the difference between the ADC input

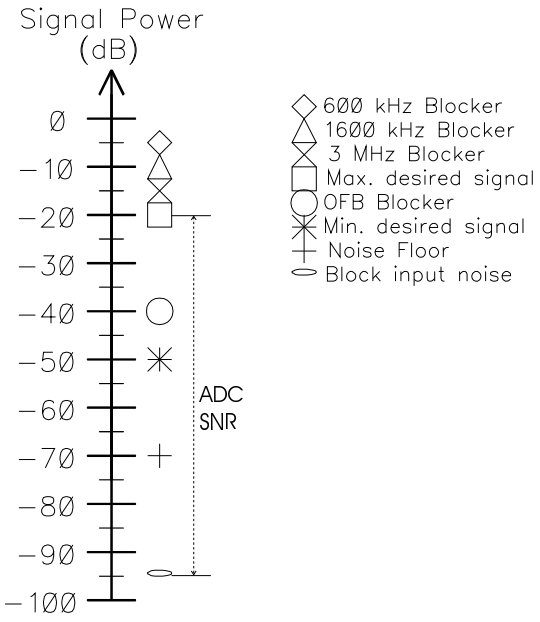

Figure 4.9: Specification of the ADC SNR for GSM signals.

noise power and the maximum desired signal power is also marked. As it can be seen this difference is roughly 74 dB plus the 6 dB circuit noise margin we have a 80 dB *SNR* requirement for the ADC when the receiver is operating in GSM mode.

As mentioned, for the UMTS standard a Zero-IF architecture is going to be used. Because the signal BW is 3.84 MHz and the existing safety margin of 1.16 MHz produces a channel bandwidth of 5 MHz, a coupling capacitor can be used to reject the DC offsets and noise by implementing a highpass function near DC as in previous approaches. The baseband filter, that should select the desired channel, is a lowpass with a corner frequency of 2.5 MHz and should exhibit good linearity because it should attenuate large interferers or blockers accompanying a weak desired signal without creating in-band spurious tones. For this filter the most convenient implementation would be offered by an active g_mC realization. The remaining blocks (VGA and ADC) will be shared with the GSM and BT receivers. The signal power levels at the input of the ADC are traced in figure 4.10; from that graphic it is found that the ADC required *SNR* including the 6 dB safety margin is about 56 dB.

The requirements imposed by the BT standard are less restrictive in comparison with the other two standards. For this receiver, the RF interface contains only an RF switch and the band select filter. Due to the low noise figure required, the requirements of the LNA an Mixer are relaxed. The image rejection filter must assure an image attenuation of 20 dB, while the channel selection requires a rejection of 40 dB at 3 MHz offset from the passband. These filters can be realized using a passive RC-CR implementation, consuming a very low or no power at all. AGC and ADC are still being common blocks of this receiver. The *SNR* derivation for the ADC is

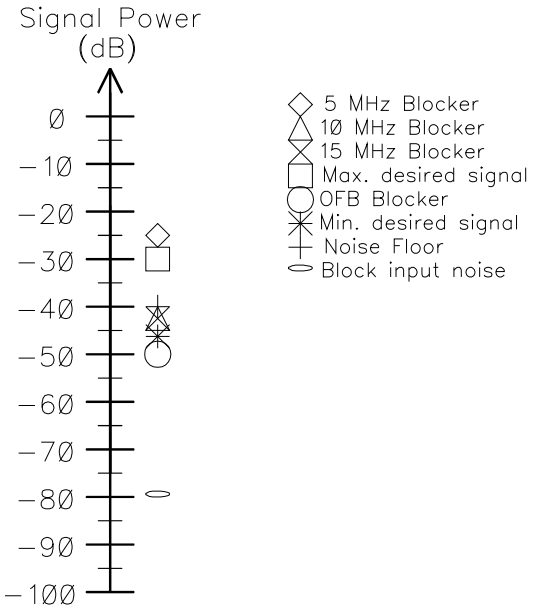

Figure 4.10: Specification of the ADC SNR for UMTS signals.

accomplished from the resulting power level profile given in figure 4.11, it can be observed, that around 58 dB would fulfill the required resolution.

4.6 Summary

Up to the point of writing this thesis, the architectures used to design a multi-standard wireless receiver were reviewed in this chapter. As it can be concluded, the problem of sharing the hardware resources in an efficient way is probably the most critical one by designing a DSMP. Every approach has in common the usage of separate RF interfaces after the antenna; this is a direct consequence of the different RF bands assigned to each standard and it seems to be unavoidable to have them unshared. IF filters have to be separated as well, unless every standard managed uses the same IF as in the second architecture presented here, however, special care should be taken by choosing the value of IF and its relationship to the sampling frequency f_s if the time offset problems already mentioned want to be avoided. Of course a trivial solution would be to chose the IF to be zero but the very well known problems with DC offsets make this election a prohibited one for narrow band standards as GSM. As a good compromise the proposed architecture as well as the third one presented use zero IF for wideband signals and low IF at BW/2 for narrow band systems. However, in the proposed approach the hardware resources sharing at the RF front end is more efficient because both the I and Q paths are being digitized and the IF filters also play the role of image rejection filters. ADC's based on sigma-

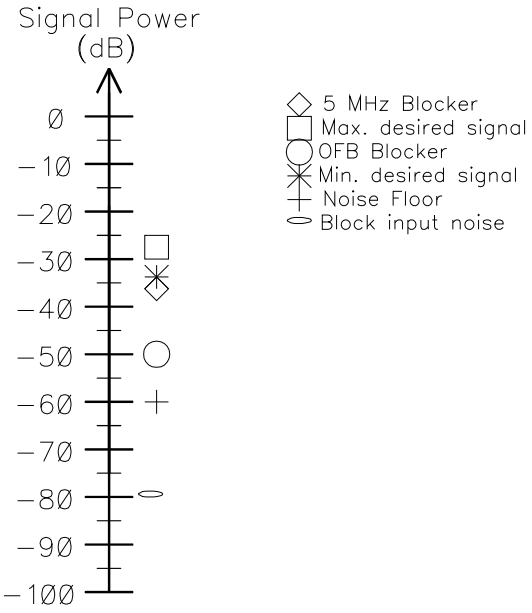

Figure 4.11: Specification of the ADC SNR for BT signals.

delta modulators are the best election in each case, because according to the theory presented in chapter number three, they have the characteristic of having a variable resolution according to the elected sampling rate without changing the architecture. This fact has been exploited by the designers of the presented multi-standard reception methods and will be subject of study in the next chapter, where the system design of the multi mode ΣΔM required by the developed receiver is going to be addressed.

Chapter 5

System Design of a Tri-Mode Sigma Delta Modulator

Contents

5.1 Introduction

In this chapter, the system level, also called architectural level, design of the proposed tri-mode sigma-delta modulator is presented. At this level of abstraction, important decisions having a

later impact in the performance of the implemented circuit are met by the designer. For this reason, system level design is a very important task that should be carried out in an iterative manner if there is an interest in achieving an optimal solution. Architectural level design is assisted by behavioral simulators, these kind of simulations help the designer to verify whether the developed system satisfies the imposed requirements at this early design phase. The non-linear nature of each ΣΔM, which is due to the presence of the hard quantizer embedded in the loop, makes the usage of behavioral simulations a mandatory step in the high level design of this systems. As stated, modelling of the hard quantizer using a linear element, namely an additive white noise source, reduces significantly the analysis of theses systems. However in design tasks, using the mentioned linear modell does not help to ensure that the final non-linear system preserves the stability characteristics predicted or exhibited by the equivalent linear system and so, stability of a designed noise shaping loop must be proven by means of exhaustive high level simulations. The discussion here starts with the set of specifications derived in the last chapter and a first design space exploration. The two possible realization methods of ΣΔ modulators are also presented and discussed. After that, the most important architectural choices can be found, analysed and their suitability for a reconfigurable solution compared. After that architectural analysis, the adopted solution is presented and the design of the NTF and STF that fulfill the requirements as well as the stability criteria is carried out. As it is going to be pointed out, in order to decrease the sampling ratio and to increase the resolution, the zeros of the NTF have to be moved from the origin and to be placed within the BW of interest. This is accomplished using resonators in the implementation of the chosen architecture. The realization of switched capacitor (SC) resonators which central frequency is located at f_s/n has been carried out using mainly two forms: based on integrators and based on delay cells. These two methods of synthesis are presented and carefully examined. The conducted analysis shows the superiority of integrator-based topologies. Such an analysis has not been reported in the literature for the case of resonators at f_s/n, thus being a contribution of this work as well. Finally some conclusions are given.

5.2 A/D Converter Specifications

After the analysis conducted in the previous chapter, table 5.1 summarizes the requirements imposed to the ADC in each mode of operation.

It can be observed that the GSM mode of operation is the one that imposes the most stringent requirements concerning SNR, it is in contrast the one with the narrowest BW. On the other hand, UMTS possesses a wide signal spectrum comprising around 4M Hz and asking for almost 10 bits of resolution. Placed in the middle concerning BW requirements, the BT standard is encountered, in this case signals with 1M Hz have to be converted also with a resolution of

Mode	GSM	UMTS	BT
SNR (dB)	80	56	58
BW (Hz)	200k	3.84M	1M
IP3 (V_{rms})	20	20	20

Table 5.1: ADC Requirements

10 bits. In [13] a derivation of the linearity requirements of the ADC in each operation mode was also carried out, the election of the elements in the RF front end of each standard was such that the linearity needed is the same for every case. In that work, the linearity measurement was expressed in terms of the two tone test parameter $IP3$ (*third order intercept point*). The $IP3$ characterizes the linearity of the system for a small input signal accompanied by strong interferers, as is the case of wireless receivers. Under such conditions, the third order intermodulation terms of the interferers overlay over the desired signal, being so impossible to filter and therefore diminishing the *SNR*. The $IP3$ is defined as the signal level at which, the amplitude of the third order intermodulation terms become equal to that of the fundamental in a two tone test. Thus, the $IP3$ point may be found as:

$$A_{IP3} = \sqrt{\frac{4 \times a_1}{3 \times a_3}} \tag{5.1}$$

Where a_1 is the linear term and a_3 the third order distortion coefficient. With this definition and the given values of $IP3$ it follows that the spurious signals created by the interferers must be at least 50 dB bellow the desired signal.

There are many open questions concerning architecture, internal resolution and *OSR* when starting the design procedure of a $\Sigma\Delta$ modulator. As stated in the introduction, the design procedure of $\Sigma\Delta$ modulators is an iterative process and hence there is no direct answer to the questions of what is the correct architecture, the optimized sampling frequency, or the quantizer resolution. Regardless of the selections adopted, however, there are some design aspects, defined by the application, which help the designer to take the better solution. For the present problem, the requirement of flexibility, which arrives from the fact of having a multi-standard converter, should be also taken into account by evaluating the candidate architectures. These topics are subject of the next discussion.

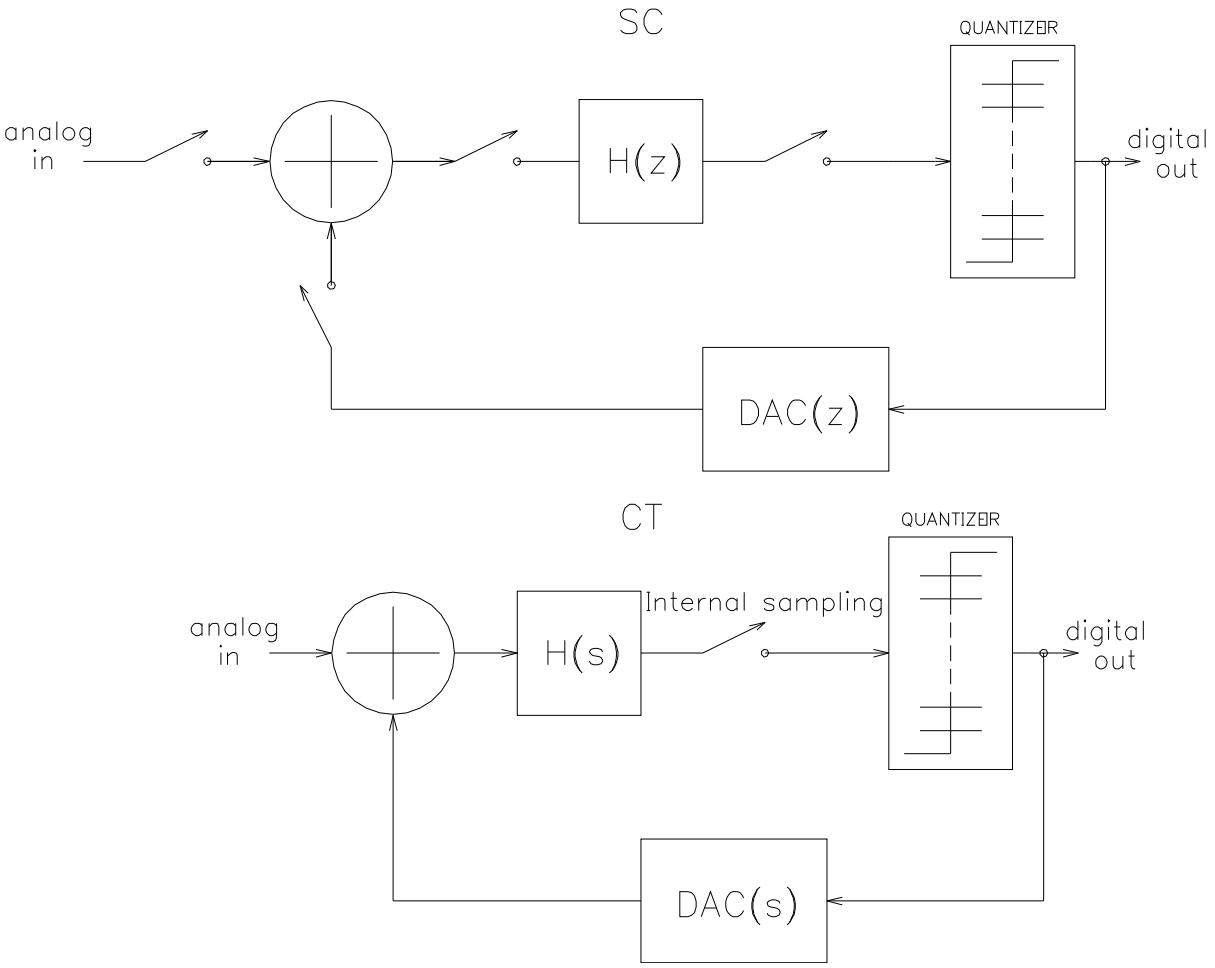

Figure 5.1: System level implementation of SC and CT ΣΔ modulators

5.3 Realization Methods

Perhaps the first choice that must be made in designing any ΣΔM is a selection between a SC implementation and a conventional active-RC (continuous-time) design. Figure 5.1 shows the system level implementation of both circuit styles.

Continuous time (CT) realizations have the advantage that an anti-alias filter can be avoided reducing so the power consumption [2,3]. On the other hand, discrete time realizations have a higher *Q* factor [3,4], this fact allows to reduce the order of the modulator to reach the same *SNR* as a continuous time counter part, helping to ensure stability. Another practical disadvantage exhibited by most CT filters is their relatively poor linearity and noise performance. Although SC filters have been realized with linearities better than 90 dB, CT filters have distortion plus noise performance not much better than 60 dB, but very often it is much worse [40]. Probably the most important problem of CT ΣΔM's is clock jitter, due to the presence

Realization	Advantages	Disadvantages
SC	Easy to Simulate	Large capacitors for high SNR
	CMOS compatible	Require an AAF
	Insensitive to CLK jitter	RC isolation circuits are required
	Insensitive to shape of op. amp. settling	Very difficult to prototype
	Pole, zero locations set by high accurated capacitor ratios	
CT	Easy to breadboard	No good CMOS compatibility (large capacitors, large linear resistors and low noise op. amps. are needed)
	No AAF is required	Requires accurate RC time constants
	No RC isolation circuits are required	Highly sensitive to CLK jitter
	SNR is not limited by capacitor size	Loop filter not scalable with CLK frequency
		Require high-linearity op. amps.
		More difficult to simulate

Table 5.2: Comparison of SC and CT ΣΔM Implementations

of a switching element before the quantizer. This brings time uncertainty in the feedback that raises the noise floor at the frequency of interest. For this reason the jitter specifications are always more stringent in CT designs than in their SC counterparts. Due to their potential in the field of high-speed, low-power applications, many efforts have been done to overcome the clock jitter problem present in CT implementations [41]. However, the future applications will require higher input frequencies, and clock jitter will start to limit the performance of SC ΣΔM's as well and this will be a more and more serious problem, leaving an open field for further investigations. Table 5.2 summarizes the main differences of CT and SC implementations of ΣΔ modulators [42].

Discrete time realizations of ΣΔ modulators have been done both in voltage and current domain using in each case, SC or switched current (SI) techniques. SI techniques posses a fully compatibility with standard low cost digital CMOS technology since no capacitors are needed, however the performance of the ΣΔM's realized using SI techniques is below of their SC counterparts even if they were realized using non linear capacitors [43]. After this discussion it should be clear why a SC realization of the proposed converter has been adopted for the present application requiring high linearity and high resolution. Many open questions remain concerning the final implementation and elect *OSR* for each operation mode. The next section treats the main architectures of SC ΣΔM's in order to find the most appropriate for the present purposes.

5.4 Architectural Choices

There are many architectural methods used in the design of ΣΔ modulators. They can be roughly classified in *single bit, multi bit* and *cascaded architectures*, all of them have been successfully used for the realization of ΣΔ ADC's. Every architecture has strengths and weaknesses concerning stability, required *OSR*, linearity and tonal behavior. The next discussion presents a brief comparison of these architectures trying to make emphasis in their suitability for multistandard operation. A detailed comparison of theses architectural methods can be found in [42].

5.4.1 Single Bit

Single bit architectures can also be divided in *low order single bit loops* enclosing modulators with a loop filter of order $n \leq 2$ and *high order single bit loops* with $n > 3$. The first and second order ΣΔ modulators analyzed in sections 3.4.2 and 3.4.3 belong to the first class of modulators. Low order loop modulators have the remarkable advantage of being inherently stable. Their system and circuit design is simple in comparison to all other architectures and they exhibit a good robustness against circuit implementation impairments. However, due to the low order filtering of the quantization noise, the signal and quantization error are strong correlated, leading to idling tones. As exposed in chapter three, first and second order ΣΔM's require a high *OSR* if high *SNR* is needed, limiting their application to narrow band signals in order to avoid excessive f_s and power consumption. The premise given in section 3.4.3 concerning *OSR* and *SNR* is actually true, and high resolution has been reached with moderate sampling frequency using *high order* ΣΔ *modulators* after the stability problems displayed by this family of noise shapers have been overcome.

Equation 3.21 shows that a single bit *n*-order ΣΔM with the architecture of figure 3.12 has a NTF equal to $(1-z^{-1})^n$ for such a system the gain at $f/f_s = 1/2$ equals to:

$$|NTF(z)| = \left|1 - \exp^{-\pi j}\right|^n = 2^n \tag{5.2}$$

Thus, for a fourth order modulator such a high gain results in self excited oscillation of the modulator. Therefore, the out of band gain of the NTF at $f_s/2$ has to be limited in order to stabilize the modulator. This conducts to the modification of the basic *n*-order architecture depicted in figure 3.12, to allow the synthesis of other family of NTF's having limited gain at $f_s/2$. Many topologies have been proposed to accomplish this, but the investigation conducted by Botteron et. al. [44], [45], [46] showed that adding a forward path from every integrator output to a summation node before quantization introduces a damping that has an stabilizing

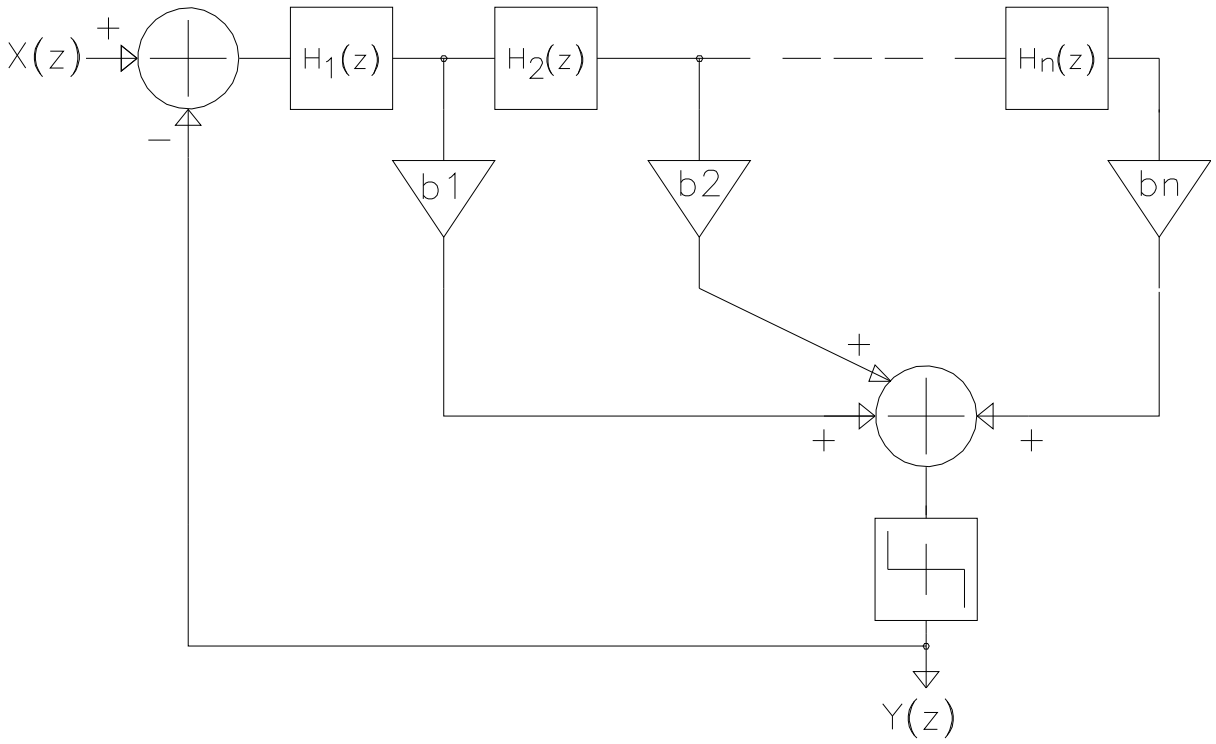

Figure 5.2: Architecture of a single bit ΣΔM with cascaded elements and feed forward coefficients

effect. The addition of coefficients to those forward paths enables the designer to manipulate the NTF in order to meet the stability recommendations given in [47]. In its general form, the architecture proposed in [44] is shown in figure 5.2

Provided that a defined design procedure handling the stability issue exists [48], single bit high order ΣΔM's become very attractive because they are able to reach high values of *SNR* for modest *OSR*'s and their circuit implementation is very robust. Single Bit modulators own also the highest linearity of all architectures and simplifies a lot the design of the DAC embedded in the feedback path. Two level quantization avoids the need for matched quantization level spacing. Threshold level and hysteresis of the comparator performing the quantization are not critical. Due to the randomization experienced by the quantization noise in high order single bit loops, idle tones are a minor problem in this kind of converters. Multi-mode operation of a converter designed with such an architecture would offer two alternatives: Using the same loop filter for every BW managed, observing that the required *OSR* to achieve certain *SNR* does not produce an excessive sampling rate, or to design a filter loop optimized for every BW and resolution. In this last case, if the order of the filter is maintained, the change in the operation mode would suppose to change the coefficient set, which is implemented by capacitor ratios, however, the operational amplifiers needed for the SC realization could be reused.

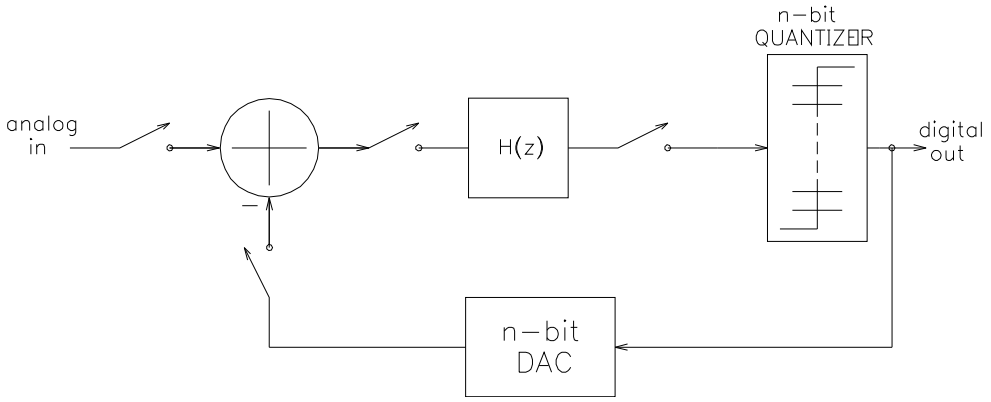

Figure 5.3: Architecture of a multi bit ΣΔM

5.4.2 Multi Bit

Moved by the fact that adding resolution bits to a quantizer improves the *SQNR* of a system by roughly 6dB, designers have added more levels to the quantizers used in ΣΔM's, conducting this to the appearance of the so called *multi bit architectures*. Figure 5.3 shows a generic architecture of a multi bit ΣΔ modulator. Thus, equation 3.23 can be modified to account for the presence of any additional bit of resolution:

$$SQNR = 10\log\left(\frac{6\times(2n+1)\times OSR^{2n+1}\times A^2}{\pi^{2n}\Delta^2}\right) + 6.02(B-1) \tag{5.3}$$

In principle, multi bit architectures allow reaching high *SNR* for fairly low *OSR*'s. The stability is much easier to achieve since low order loops can still being used for a more spread range of *SNR*'s. Even in high order loops, stability is improved because the finer quantization error requires lower signal swing in the operational amplifiers. Further, the extra quantization levels randomize the nature of the quantization noise reducing the idle tones. However, the advantages of having multiple bit quantizers cannot be completely exploited because the linearity requirements imposed to the internal DAC are very severe. Unfortunately, the linearity of the n-bit DAC limits the achievable linearity of the whole converter. Any distortion or DC offset introduced by the DAC adds directly to the signal path without shaping and degrading so the performance of the whole converter. Autocalibration or dynamic element matching techniques can reduce these effects, but at the expense of more circuitry and power consumption. Concerning reconfigurability, these family of modulators could be exploited by using a programmable quantizer which adds bits of resolution when needed in order to conserve a moderate f_s for every considered BW, although this solution would conduct to a non-optimal hardware resource sharing because it implies connection or disconnection of some comparators in the quantizer plus the error correction circuitry.

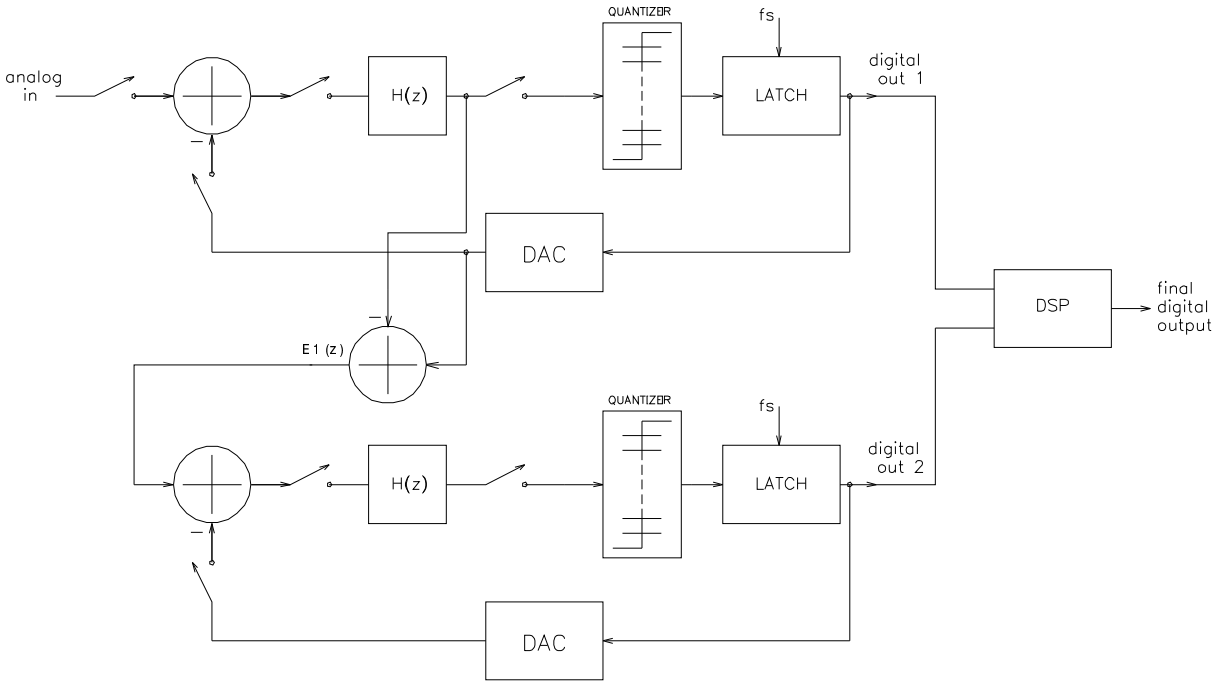

Figure 5.4: Architecture of a generic two-section cascaded ΣΔM

5.4.3 Cascaded

Another method to design stable high order ΣΔ modulators consists in connecting low order sections in cascade, obtaining so the desired high order modulator. Since first and second order noise shaping loops are unconditionally stable, the entire system shows also the same stability property. A system level diagram of a cascaded ΣΔ modulator consisting of two sections is shown in figure 5.4

As it can be seen, in this class of modulators, the input of the second section is an estimation of the quantization error of the first loop. The output of every single modulator is fed to a DSP block, whose function is to add both digital output signals and to cancel the error coming from the first noise shaper. Thus, if the function $H(z)$ of figure 5.4 is $z^{-1}/1-z^{-1}$ then the output of each section is:

$$Y_1(z) = z^{-1}X(z) + \left(1-z^{-1}\right)E_1(z) \tag{5.4}$$

$$Y_2(z) = z^{-1}E_1(z) + \left(1-z^{-1}\right)E_2(z) \tag{5.5}$$

where $E_1(z)$ and $E_2(z)$ are the errors introduced by the first and second modulator respectively. The digital correction network will cancel the first stage quantization error and will produce the signal:

$$Y(z) = z^{-2}X(z) - \left(1 - z^{-1}\right)^2 E_2(z) \tag{5.6}$$

The noise coming from the first stage is digitally removed while the noise from the last stage is second order shaped. In this way, the cascade of two first order modulators provides the same noise shaping as a second order modulator. A cascade architecture resembles the operation of an N-step converter where both coarse and fine converters are $\Sigma\Delta$ modulators. Because of the preserved stability properties while constructing high order loops, this kind of modulators are also able to reach high *SNR* with modest *OSR*, thus being attractive for wide band applications in wired telecommunications such as ADSL. However, digital error cancellation relies on the supposition that the transfer function of the analog integrator of the first noise shaper is known. Analog imperfections such as leakage or gain errors present in the implementation of the elements comprised by the first stage, introduce deviations from the ideal integrator transfer function $(z^{-1}/1-z^{-1})$ leading only to a partial noise cancellation. Thus, a cascade modulator requires very good analog components difficult to design in sub-micrometric technologies and is so more sensitive to operational amplifier non-idealities than corresponding single loop modulators. Reconfigurable operation of this kind of modulators would require to find out the required order to reach the *SNR* needed in each mode without compromising the *OSR*, otherwise, changing the order of the system would suppose to have idle components in a certain mode of operation.

After this discussion it should be clear that the most convenient architectural option is offered by the *Single Bit High Order Loops*. They are still the most widely used in practice and have the least overhead for the circuit realization of the quantizer and A/D converter in both circuit area and power consumption. They also have the interesting characteristic of synthesizing different types of NTF's by changing the filter coefficients, which in turn are passive components, without altering the modulator structure, leaving the active circuit elements ready for their reemployment. The next section presents the architectural level design of the proposed tri-mode converter.

5.5 Signal and Noise Transfer Function Design

There are also many questions that have to be observed by choosing a NTF that produces a stable and at the same time realizable, high order single bit $\Sigma\Delta$M. These primary aspects are covered by stability constraints and causality constraints. Causality and SC implementation are closely related, because in principle it is not possible to realize in SC any "delay-free" branch.

Thus, the loop around the quantizer cannot be delay-free, and $H(z)$ must be strictly causal, that means, the independent term of the numerator of $H(z)$ must be zero, in other words:

$$\lim_{z\to\infty} H(z) = 1 \tag{5.7}$$

This constraint also implies, $H(z)$ cannot be forced to zero everywhere. Keeping it small in-band tends to increase it above unity out-of-band. Stability is a harder problem, making the linear model of the modulator stable does not guarantee that the real nonlinear system remains stable. There is lack of a complete theory on stability adequate for design, but as explained in section 5.4.1 what we have is an empirical method developed with the time and based on rules of thumb. The method exposed in [48] recommends a maximum out of band gain at $f_s/2$ of 6 dB in order to maintain stable a loop comprising a single bit quantizer. This means:

$$|NTF(\exp j\pi)| < 4 \tag{5.8}$$

Then, given the *BW*, *SNR* and the constraints imposed by 5.7 and 5.8, loop filter design is a trade-off among sampling rate, filter order and *SNR*. With certain modifications, which are going to be addressed later on, it is possible to use a highpass Butterworth or Chebyshev of second kind filtering functions for the design of a NTF that fulfils the requirements stated in the last two equations. However, an initial guess is necessary as starting point for the design of an adequate NTF. In this sense, the *SQNR* produced by eq. 3.23 could be used as a crude approximation in order to estimate the required f_s for modulators of different orders delivering the same resolution. Figure 5.5 shows a graph of *SQNR* vs *OSR* for loop orders ranging from 2 to 5.

It can be seen that the same *SQNR* can be reached with lower *OSR* for increasing order of the modulator loop. As example, in order to have a closed number of bits, the required resolution in each operation mode of the modulator under design is going to be managed as 84dB or 14 bit for GSM and 10 bit or 60 dB for both UMTS and BT. For the following discussion the *SNR* required by GSM will be taken because it is the most stringent. From graphic 5.5 it is found that *OSR*'s of 10 and 60 are required to achieve the $SQNR = 84$dB for modulators of order 4 and 2 respectively. Knowing the *BW* of the GSM signals, sampling frequencies of 4 MHz and 24 MHz are obtained. As a coarse approximation and having in mind the SC implementation of the modulator, the required bias current of the operational amplifiers can be estimated according to the slew rate needed in each case. It is well known, that the election of the capacitor size in a sample and hold circuit that will be used in an ADC is established by the so called kT/C noise and the number of bits, which are related by:

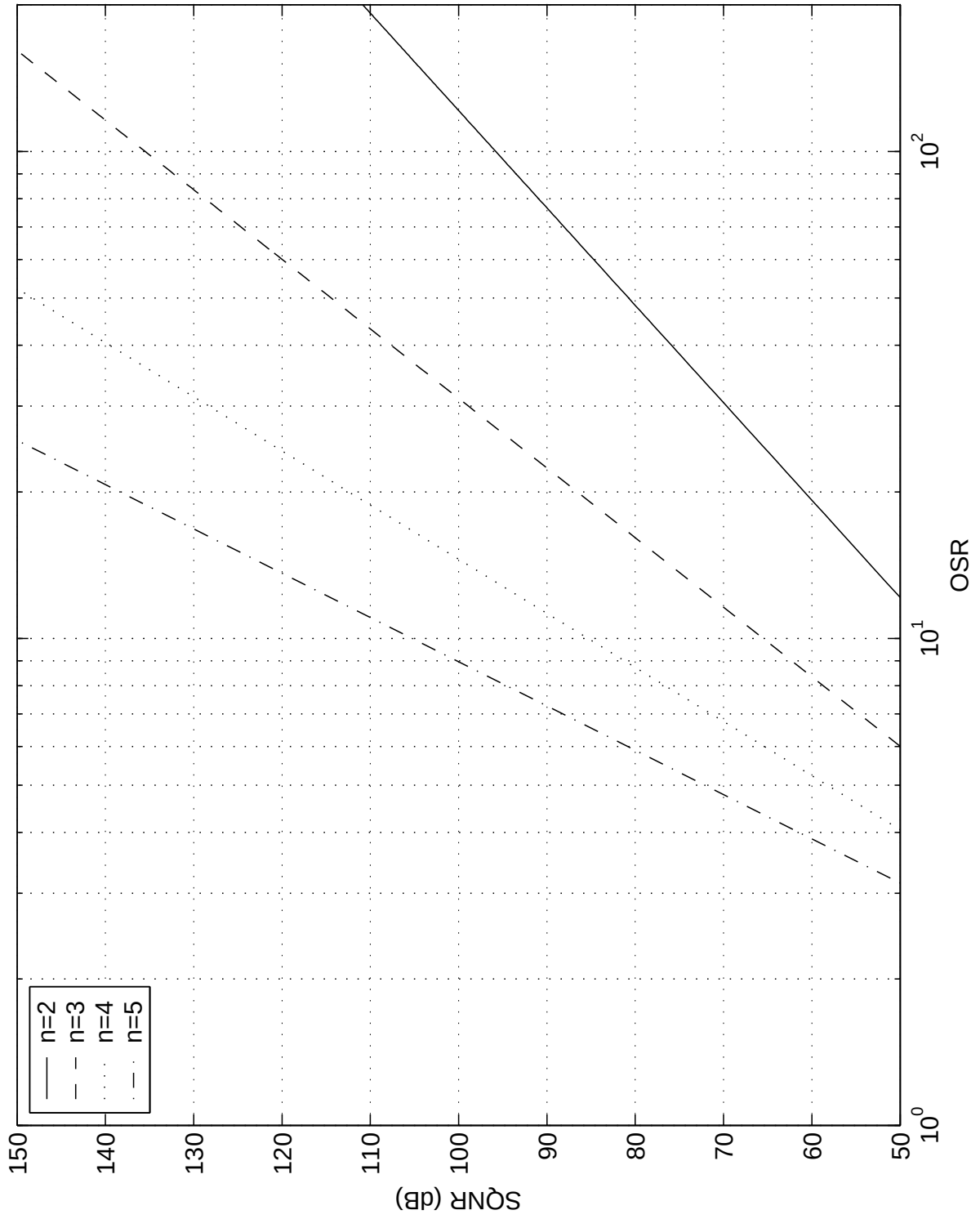

Figure 5.5: *SQNR* vs *OSR* for loop orders ranging from 2 to 5.

order	OSR	f_s	t_{set}	SR	I_{Bias}	P_{diss}
2	60	24MHz	20.83ns	158.5V/μs	158.5μA	1mW
4	10	4MHz	125ns	26.4Vμs	26.4μA	348μW

Table 5.3: SR and power consumption requirements for 2nd and 4th order modulators

$$C \approx \frac{kT \times 12}{2^{-2N} V_{REF}^2} \tag{5.9}$$

where N is the number of bits, V_{REF} the voltage corresponding to the ADC full scale, k the Bolltzmann's constant and T the absolute temperature. For 14 bits the last equation produces a capacitor of value $C \approx$ 1pF for a full-scale voltage of 3.3V. Using these parameters, table 5.3 summarizes the available settling time, SR, required bias current per op. amp and estimated power consumption for the cases under consideration. It was assumed that single stage operational transconductance amplifiers are going to be used in the implementation. It can be observed that a reduction of around 60 percent in the power consumption can be attained if a 4th order modulator is used.

Although these results should be taken with care, because there is a tremendous decrease in attainable SNR for modulators having a NTF constrained by the stability criterion, they can be used as a first step. Another reason for choosing a 4th order loop is the possibility of using two resonators in the loop in order to move the zeros of the NTF from zero to the optimal positions recommended in [47]. The graphics of the performance shown in that paper, present the result of SNR versus OSR for different modulator orders, whose zeros were moved to their optimal positions. Those results are useful to minimize the OSR required to reach a moderate SNR in wideband applications, as is the case in the BT and UMTS operation modes. The mentioned paper shows that a $SNR = 60$dB is reached by a 4th order $\Sigma\Delta$M with an $OSR \approx 20$ if the zeros are split. The UMTS standard requires for the highest f_s because it has the wider band, and with the elected order, the sampling frequency required equals 76.8MHz, as only half of the total BW has to be converted. This is also a reasonable value for the target technology characterized by a minimum channel length of 0.3μm.

After the election of the order of the loop filter has been accomplished, we are in conditions of finding out the appropriate NTF. The procedure described in [48] for the design of NTF's based in highpass Butterworth filtering is summarized below:

- Using any commercial digital filter design tool find a Butterworth highpass filter, which highest order z coefficient C_n has a value between 0.7071 +/- 10% as required by the stability constraints, since the gain at $f_s/2$ will be $1/C_n$

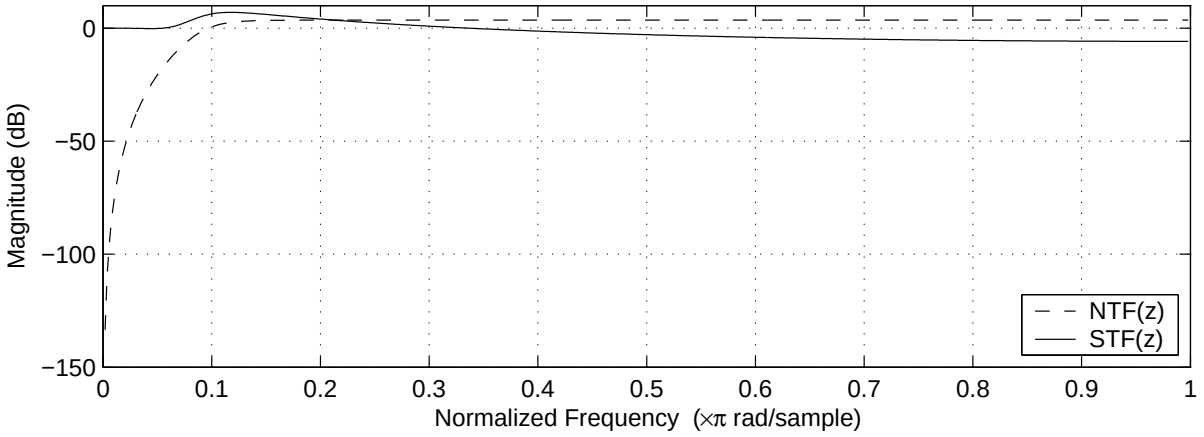

Figure 5.6: Designed NTF and STF.

- Normalize the numerator of the found filter by C_n. This ensures that the found function obeys the causality constraints.
- Find the loop filter $H(z)$ from: $NTF(z) = 1/(1+H(z))$. The $STF(z)$ will be defined by the complementary property displayed by NTF and STF.
- Plug the obtained $H(z)$ into a discrete tiem simulator and verify if the nonlinear system remains stable by observing the noise shaping, further simulations can be performed to ascertain the stable input range and the *SNR*
- Chose a topology to implement $H(z)$ and compute the coefficients for the chosen topology.
- Simulate the modulator behavior to confirm the performance
- Scale the internal nodes to the desired swing

The first two steps usually require of several iterations to find out the proper cutoff frequency of the asked highpass filter. The fist 3 steps were carried out with *MATLAB* a graph of the final result for both the NTF and STF can be found in figure 5.6

The final NTF is given by:

$$NTF(z) = \frac{1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4}}{1 - 3.1806z^{-1} + 3.8612z^{-2} - 2.1122z^{-3} + 0.4383z^{-4}} \tag{5.10}$$

This function was plugged into *MIDAS* to simulate the non-linear loop. The undecimated spectrum of the output of the single bit quantizer is shown in figure 5.7a. Proceeding in the same

way as in section 3.5.1 with the last equation, after the substitution of z by $\exp(2\pi j f/f_s)$, carrying out the Taylor series expansion and integrating the first term of the series, the approximated value of P_e is given in eq. (5.11). Using this result, approximated expressions for the *SQNR* and *DR* are found in (5.12) and (5.13). According with those expressions, a $SNR \approx 96$dB could be reached with an *OSR* of 40 and $\Delta = 3.3$. Simulations, as shown in figure 5.7b, confirmed these estimations.

$$P_e \approx \frac{2.5\pi^7\Delta^2}{OSR^9} \tag{5.11}$$

$$SNR \approx \frac{A^2 OSR^9}{5\pi^7\Delta^2} \tag{5.12}$$

$$DR \approx \frac{OSR^9}{20\pi^7} \tag{5.13}$$

The presented NTF will be used for the GSM mode, as it requires the highest *SNR* and has the narrowest *BW*. As mentioned, in order to reduce the sampling ratio, which is more critical in the UMTS mode because of its wider band signals, two zeros are going to be moved from DC and put at positions recommended in [47]. The final ΣΔM will be implemented using the architecture depicted in figure 5.2. That topology produces complementary signal and noise transfer functions. In its general form, the STF and NTF are given by:

$$STF(z) = \frac{\sum_{i=1}^{n} b_i H(z)_i \prod_{i=2}^{n} H(z)_{i-1}}{1 + \sum_{i=1}^{n} b_i H(z)_i \prod_{i=2}^{n} H(z)_{i-1}} \tag{5.14}$$

$$NTF(z) = \frac{1}{1 + \sum_{i=1}^{n} b_i H(z)_i \prod_{i=2}^{n} H(z)_{i-1}} \tag{5.15}$$

If functions $H_i(z)$ have poles and zeros of the form $H_i(z) = z_i/p_i =$ where $z_i = (zero_i + z)$ and $p_i = (pole_i + z)$, the last equation can be expressed as:

$$NTF(z) = \frac{p_1 p_2 \dots p_n}{p_1 p_2 \dots p_n + b_1 z_1 p_2 \dots p_n + b_2 z_1 z_2 \dots p_n + \dots b_n z_1 z_2 \dots z_n} \tag{5.16}$$

Equation 5.16 shows how the *poles* of the elements present in the forward chain of the architecture shown in figure 5.2 set the *zeros* of the noise shaping function. As exposed in section

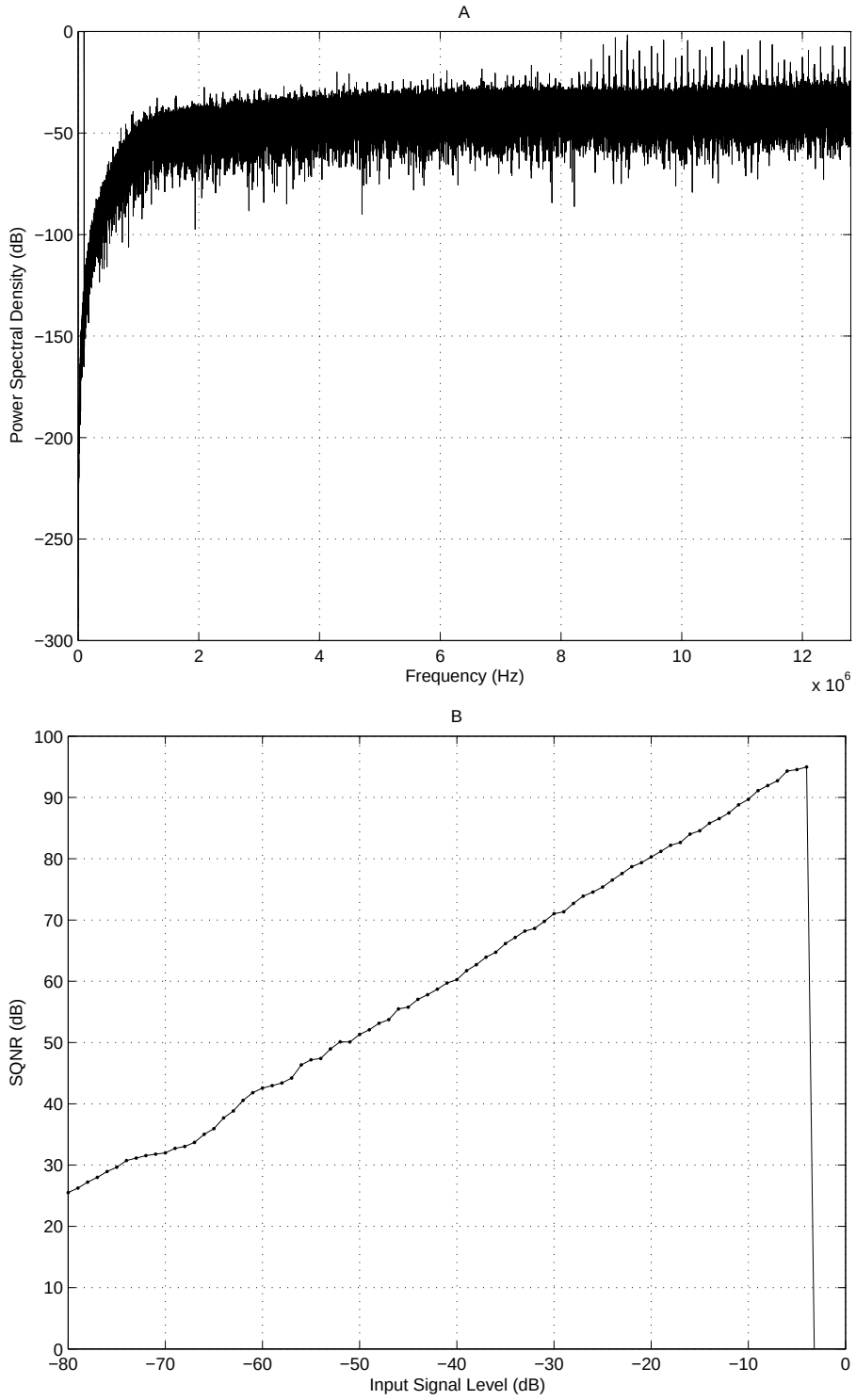

Figure 5.7: Undecimated output signal spectrum (A) and *SQNR* performance (B)of the designed NTF.

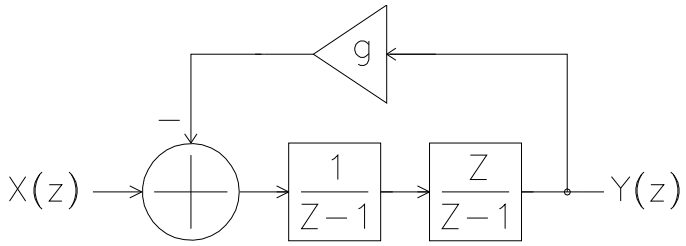

Figure 5.8: An integrator based resonator.

3.5 *resonators* are used if the poles of an element have to be placed at certain frequency. There has been a great interest in analyzing the different existing structures to synthesize resonators at frequencies around $f_s/4$ because they are the fundamental elements needed in the design of BPΣΔM's. However it is not the case for resonators at frequencies different of one quarter of f_s. The literature reports mainly two structures for the design of SC resonators at f_s/n namely, *The Integrator Based Resonator* and *The Delay Based Resonator*. These two structures are going to be presented in the next section. A detailed analysis of their robustness against the main op. amp. non-idealities is also carried out.

5.6 Switched Capacitor Resonators at f_s/n

5.6.1 The Switched Capacitor Integrator Based Resonator

A system level diagram of a SC integrator-based resonator is presented in figure 5.8. There, the classical *lossless discrete integrator* structure can be recognized. This arrangement has been used in both BP and LP ΣΔM realizations [49],[50].

The transfer function of this configuration is given by:

$$H(z) = \frac{z^{-1}}{1+(g-2)z^{-1}+z^{-2}} \tag{5.17}$$

The previous equation puts two poles located at the normalized frequency value:

$$\omega_n = \pm\cos^{-1}\left(\frac{2-g}{2}\right) \tag{5.18}$$

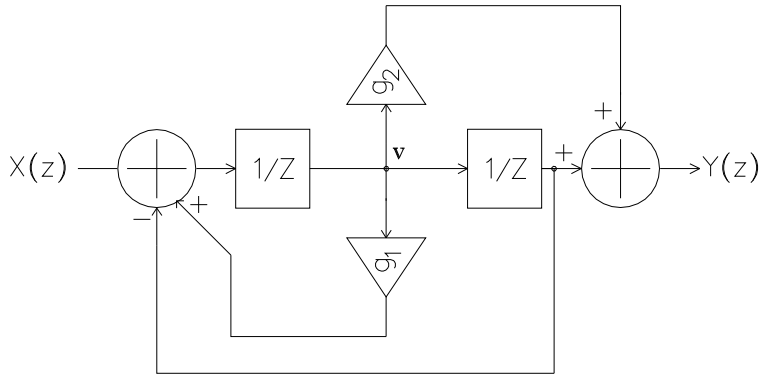

Figure 5.9: A delay based resonator.

As it can be observed, parameter g, which in turn becomes a capacitor ratio, is used to fix the desired resonant frequency, in principle at any angle ranging from 0 to π inside the unitary circle. This has been used by designers to suppress the quantization noise both at $f_s/4$ or near base band. It is well known that the characteristics of real operational amplifiers used in the realization of this resonator cause deviations from this ideal model. Those effects have been subject of extensive research, when this construction is used to implement resonators at $f_s/4$. It is not the case for resonators at f_s/n, useful to reduce quantization noise at base band. Moreover, there is another structure that uses delay elements to create resonators both at $f_s/4$ or f_s/n which analysis has been ignored, up to the point of writing this work, when used to synthesize resonators at f_s/n. Next, the mentioned construction is presented.

5.6.2 The Switched Capacitor Delay Based Resonator

Proposed in 1991 by Horrocks [9], an arrangement based on delay cells, and capable to produce resonant peaks at different normalized frequencies is presented in the next figure.

This resonator has a transfer function from $x(z)$ to $y(z)$ equal to:

$$H(z) = \frac{g_2 z^{-1} + z^{-2}}{1 - g_1 z^{-1} + z^{-2}} \tag{5.19}$$

from (5.19), if $g_1 = g_2 = 0$ the transfer function collapses to $z^{-2}/(1+z^{-2})$, which is the transfer function of a resonator at $f_s/4$. This is in fact a very often used form to synthesize resonant elements at one quarter of the sampling frequency, that has been deeply analyzed because of that interesting and useful property for IF digitization [4],[51]. Horrocks used the same structure for resonators at $0.1\,f_s$. Recently [10], the usage of this array was proposed to produce resonators at

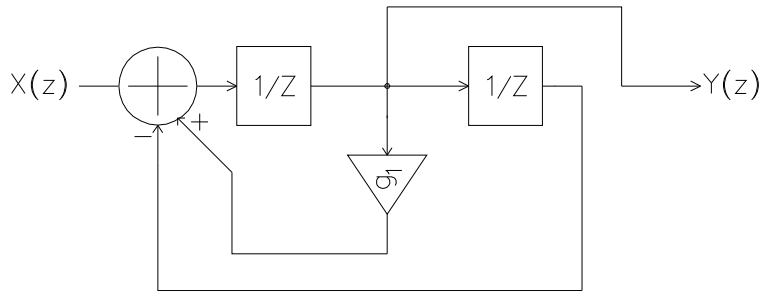

Figure 5.10: A delay based resonator at f_s/n.

$0.0718\,f_s$ and $0.4282\,f_s$. There is however a lack of analysis of the sensitivity of this resonator to the imperfections of its SC implementation, when it produces frequencies different from that at $f_s/4$, as well as a comparison with the classical integrator based construction used also at f_s/n.

From (5.19) if $g_2 = 1$ and the output is taken from the point marked as v in figure 5.9 it can be shown that the transfer function becomes:

$$H(z) = \frac{z^{-1}}{1 - g_1 z^{-1} + z^{-2}} \tag{5.20}$$

Thus, a delay based resonator at f_s/n, whose central frequency is controlled by a single parameter g_1 is shown in figure 5.10.

This resonator has also two complex conjugated poles of radius 1, positioned at normalized frequencies given by:

$$\omega_n = \pm \cos^{-1}\left(\frac{g_1}{2}\right) \tag{5.21}$$

This permits to fix the resonant frequency at any angle between 0 and π as well.

In order to analyze the effects produced by operational amplifier non-idealities over these pair of resonators, the SC implementation of their building blocks, namely a SC integrator an a SC delay element is going to be reviewed. In the next discussion as well as in the remaining of this work it is assumed that every operational amplifier present in the implementation is an operational transconductance amplifier (OTA). The impairments that will be considered are finite voltage gain (A_V), non zero input capacitance (C_{in}), finite unity gain frequency (f_u) and capacitor mismatch. For the sake of simplicity, their effects were considered separately following an analysis method similar as that found in [52].

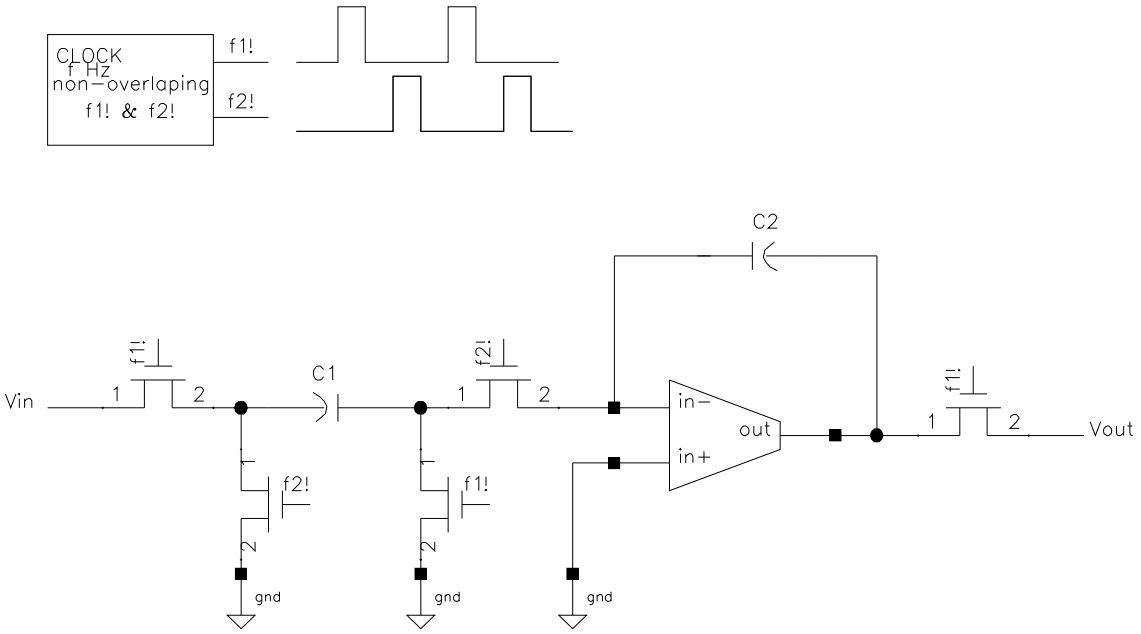

Figure 5.11: SC Integrator.

5.6.3 The Switched Capacitor Integrator

The classical non-inverting delayed integrator is exposed in figure 5.11. The switches are controlled by a two-phase non-overlapping clock generator as shown in the same picture. If it is assumed that the OTA is ideal, it is well known that the transfer function of this circuit is given by:

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}} \tag{5.22}$$

If the OTA used in the integrator is real with finite A_V and non zero C_{in}, when $f2!$ is on, the OTA is connected as depicted in figure 5.12 and a voltage different from zero appears at node n as indicated in that figure.

It can be shown that, the ideal transfer function given in 5.22 transforms in:

$$H(z)_m = \frac{C_1}{C_2}\frac{\varepsilon_n z^{-1}}{1-\varepsilon_d z^{-1}} \tag{5.23}$$

where:

$$\varepsilon_n = \frac{A_V\beta}{1+A_V\beta}$$

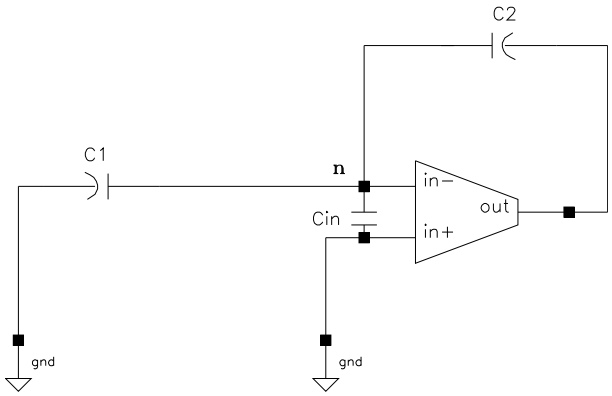

Figure 5.12: SC Integrator during charge transfer.

$$\varepsilon_d = \frac{\beta(1+A_V)}{1+A_V\beta}$$

$$\beta = \frac{C_2}{C_1+C_2+C_{in}}$$

If such an integrator is used in the loop of figure 5.8, a resonator with the following transfer function is constructed:

$$H_R(z)_m = \frac{\varepsilon_{n1}\varepsilon_{n2}z^{-1}}{1-(g\varepsilon_{n1}\varepsilon_{n2}-\varepsilon_{d1}-\varepsilon_{d2})z^{-1}+\varepsilon_{d1}\varepsilon_{d2}z^{-2}} \tag{5.24}$$

Here, error terms $\varepsilon_{n,d1}$ and $\varepsilon_{n,d2}$ account for the imperfections of the first and second integrator respectively. In equation 5.24, the products $\varepsilon_{n1}\varepsilon_{n2}$ and $\varepsilon_{d1}\varepsilon_{d2}$ introduce gain errors affecting the Q factor of the resonator, the term $\varepsilon_{n1}\varepsilon_{n2}-\varepsilon_{d1}-\varepsilon_{d2}$ modifying the ideal coefficient of z^{-1} deviates the resonant frequency to a lower value. This model was plugged into *MIDAS* and simulations of the frequency response of such a resonator were accomplished for gain values of 60, 70 and 80 dB, the chosen normalized central frequency was chosen to be $0.025 rad/s$, corresponding to a zero put at the border of the *BW* if an *OSR* of 20 is used, as will be the case for UMTS signals. For this resonant frequency, the value of g must be 24.62×10^{-3}. These simulation results are displayed in figure 5.13.

As it can be observed, the Q factor of this resonator is severely affected by low values of A_V, because it experiments the effect of two error coefficients ε_n and ε_d. The deviation in the central frequency cannot be observed with the chosen A_V values, but it exists.

Another source of error in a SC integrator made with a real OTA is incomplete settling due to finite f_u. If the integrator is assumed to settle linearly with a single-pole response, incomplete

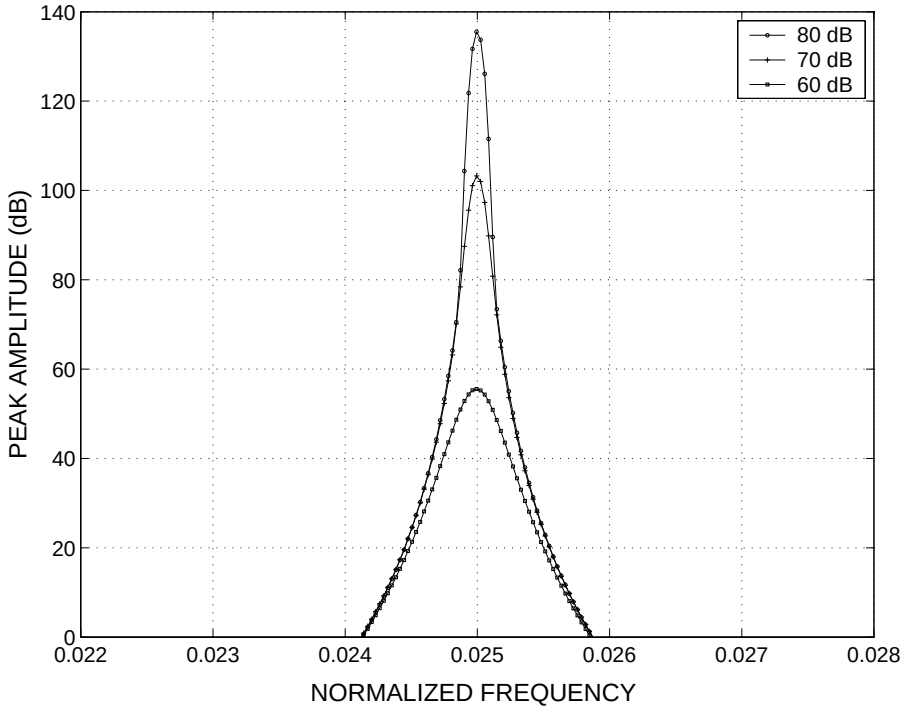

Figure 5.13: Effect of A_V and C_{in} in an integrator based resonator.

settling only manifests itself as an integrator gain error [53]. In this case, the transfer function of the integrator is

$$H(z)_m = \frac{C_1}{C_2}(1-\varepsilon)\frac{z^{-1}}{1-z^{-1}} \tag{5.25}$$

where the gain error term, ε, is:

$$\varepsilon = e^{-2\pi f_u \beta T_s}$$

Here, T_s is the time allotted for settling, and $\frac{1}{2\pi f_u \beta}$ is the closed-loop time constant of the integrator. Thus, when this integrator is plugged into the lossless discrete integrator (LDI) loop, the following transfer function is obtained:

$$H_R(z)_m = \frac{z^{-1}(1-\varepsilon_1-\varepsilon_2+\varepsilon_1\varepsilon_2)}{1+[g(1+\varepsilon_1\varepsilon_2-\varepsilon_1-\varepsilon_2)-2]z^{-1}+z^{-2}} \tag{5.26}$$

Here, ε_1 and ε_2 refer to the errors introduced by the first and second integrator, respectively. At this point, it is convenient to take a look at the SC implementation of the LDI loop. Figure 5.14 shows a fully differential implementation of this loop. There can be seen, when $f1!$ is active the first OTA has connected at its input the capacitor needed to implement the feedback coefficient, when computing the value of β_1 this capacitor comes into the denominator and lowers it, making the effect of ε_1 stronger. However, from equation 5.18 the required capacitor ratio to implement this coefficient must have a relation of 24.63×10^{-3}. With the capacitor values indicated in that figure this factor produces a capacitance of 24.63fF. The value of C_{in} was chosen to be 80fF as typical for wide transistors working in saturation with a channel length of 0.3μm. Thus, the β value of each OTA present in the implementation is given by:

$$\beta_1 = \frac{1p}{1p+1p+80f+24.63f} = 0.475$$

$$\beta_2 = \frac{1p}{1p+1p+80f} = 0.480$$

These parameters indicate that, the reduction in β_1 is about 1.0% with respect to that of β_2, this allowed to use the same values of f_u for both OTA's in the simulations of the model given in equation 5.26 and performed with *MIDAS*. Simulation results are given in figure 5.15.

The last non-ideal effect examined for this resonator was capacitor mismatch. SC circuits are very robust against variations in the absolute value of their required capacitances, because their parameters are controlled by capacitor ratios, rather than the values of a single element. For this reason the values observed in the deviation of the resonant frequency in the next results are very small, however this is also a metric that should be considered when looking for the best alternative presented for the implementation of a high performance SC system. To evaluate the sensitivity to capacitor mismatch owned by this pair of circuits, Montecarlo simulations were conducted using the *CADENCE* environment. In order to look for a closed value in the resonant frequency, a clock frequency of 160 MHz was used in the simulations. This produces a resonant peak at 4 MHz if the factor of 0.025 times f_s is maintained. Figure 5.16 shows the resulting histogram of the central frequency after 1000 Montecarlo simulations. The obtained mean frequency value was 4.0192 MHz and the standard deviation was found as 10.0942 kHz. The models used in the simulation were provided by *EUROPRACTICE* for the technology *AMS*035.

5.6.4 The Switched Capacitor Delay Element

A single-capacitor sample and hold circuit that adds a delay to the input signal is presented in figure 5.17. If the circuit is constructed with ideal elements, the transfer function is given by:

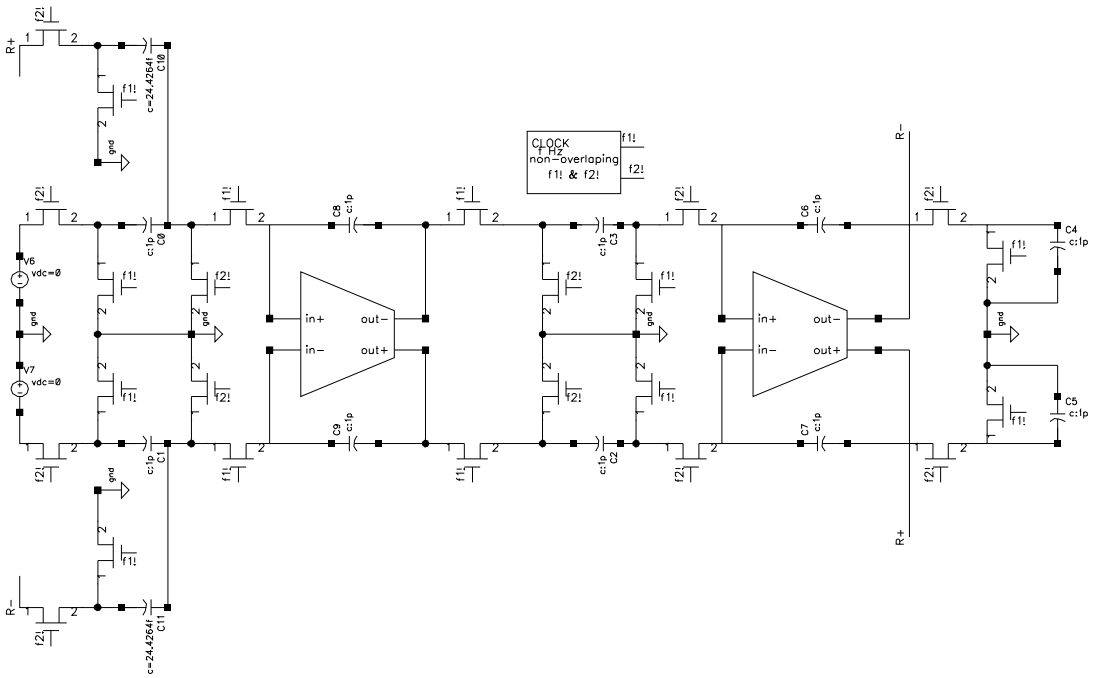

Figure 5.14: Fully differential SC implementation of a LDI loop.

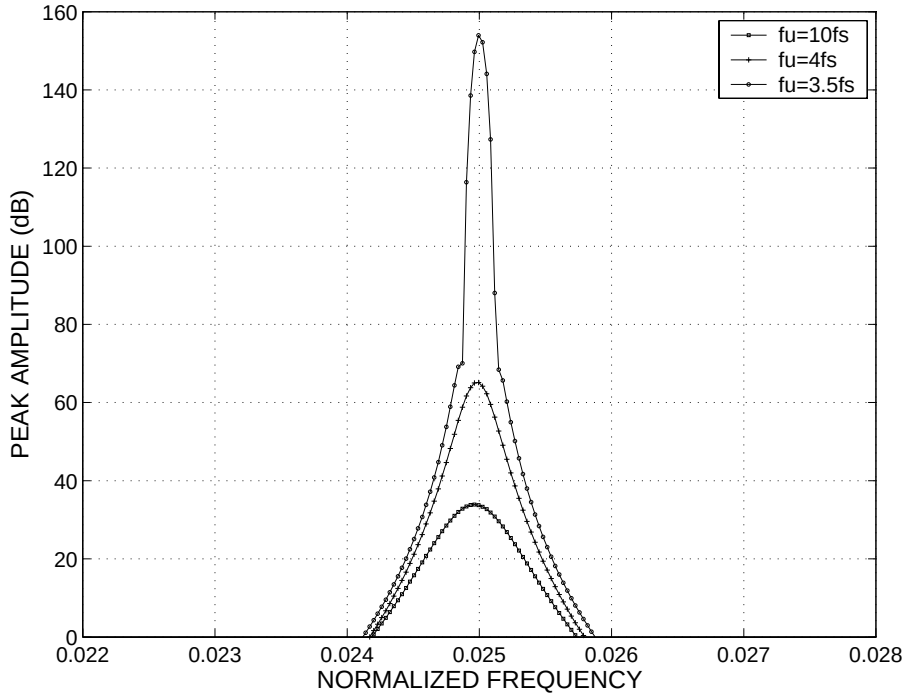

Figure 5.15: Effect of f_u in an integrator based resonator.

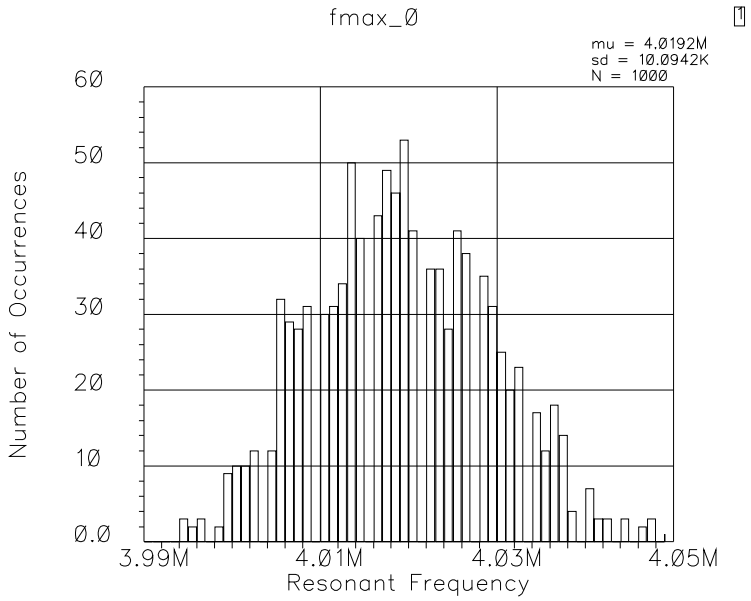

Figure 5.16: Effect of capacitor mismatch in an integrator based resonator.

$$H(z) = z^{-1} \tag{5.27}$$

In the single-capacitor sample and hold circuit, finite OTA gain A_V as well as non-zero input capacitance still causing gain error and the transfer function of the delay cell becomes [51]:

$$H(z) = \delta z^{-1} \tag{5.28}$$

where

$$\delta = \frac{A_V \beta}{A_V \beta + 1}$$

$$\beta = \frac{C_s}{C_s + C_{in}}$$

If this circuit is embedded in the loop of figure 5.10, the transfer function of a delay based resonator whose OTA's have finite A_V and non-zero C_{in} turns in:

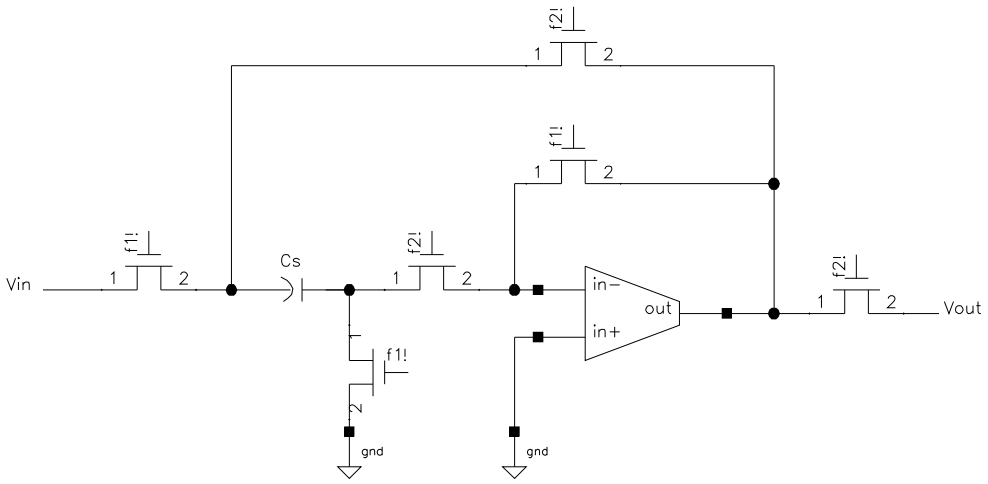

Figure 5.17: A single capacitor sample and hold circuit.

$$H_R(z)_m = \frac{\delta_1 z^{-1}}{1 - \delta_1 g_1 z^{-1} + \delta_1 \delta_2 z^{-2}} \tag{5.29}$$

After equation 5.29 it can be concluded that the effects of limited voltage gain and input capacitance different of zero in the two-delay loop are similar as in the LDI loop. Here Q degradation and deviation of the resonant frequency is observed as well. The model given in the last equation was also used in simulations performed with *MIDAS* for the same values of voltage gain as in the LDI loop and the same resonant frequency. These results are shown in figure 5.18. It is useful to compare equations 5.29 and 5.24. In 5.24 terms $\varepsilon_{d1,2}$ lead to a partial cancellation of the error introduced by $\varepsilon_{n1,2}$. This is not the case in the last equation, where the deviation of the central frequency given by the coefficient of z^{-1} directly affects the parameter g_1 with no cancellation. This in part explains the large deviation experimented by the central frequency and displayed in figure 5.18.

Looking at the SC implementation of the delay based resonator also helps to explain the observed degradation. Figure 5.19 shows a fully differential implementation of the resonator under analysis. C9 and C10 are used to implement the feedback coefficient g_1. After equation 5.21 it is found that the value of g_1 for a resonant peak at 0.025rad/s is equal to 1.9753, which produces a capacitor of 1.9753 pF in the SC implementation of this coefficient. In fig. 5.19 can be seen that, during $f1!$ C1 and C9 in the positive signal path (C2 and C10 in the negative path) are connected in parallel to the non inverting (inverting) input of the OTA. This introduces a considerable lowering in the value of β_1 which affects directly the position of the poles of the resonator. In order to have an estimation of this error the β parameter of both OTA's is calculated:

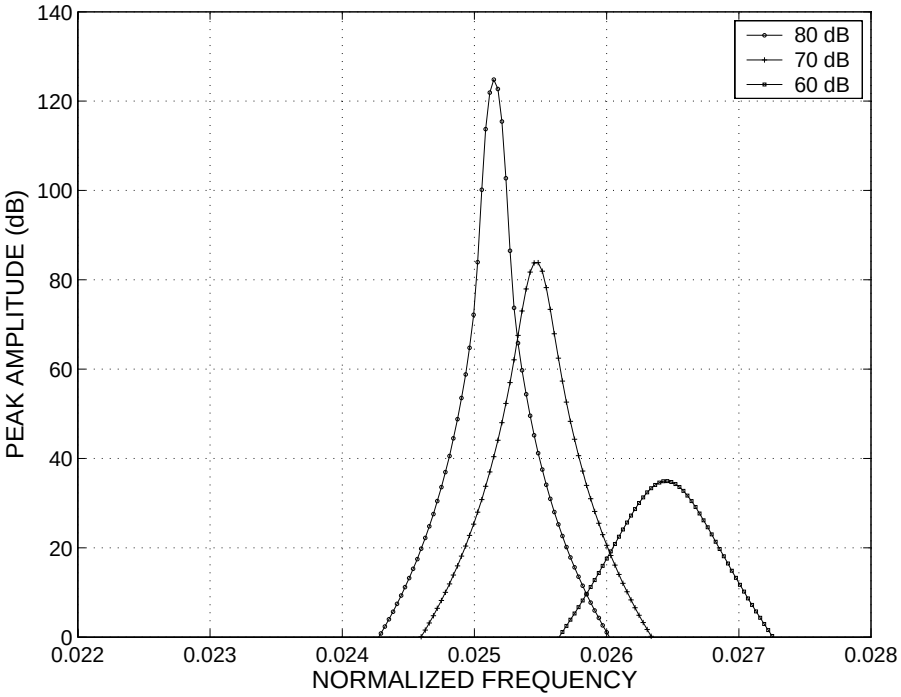

Figure 5.18: Effect of A_V and C_{in} in a delay based resonator.

$$\beta_1 = \frac{1p}{1p+1p+80f+1.9753p} = 0.2466$$

$$\beta_2 = \frac{1p}{1p+1p+80f} = 0.480$$

The reduction of β_1 is of almost 49%, this could be translated in an A_V requirement of twice higher for the input amplifier with respect to the second amplifier in order to reduce this effect.

Another source of error in the delay cell is incomplete settling of the op. amp. due to finite f_u. Finite gain-bandwidth product of the OTA's used in figure 5.17 introduces a gain error in the sample and hold circuit given by:

$$H(z)_m = (1-\gamma)z^{-1} \tag{5.30}$$

where the gain error term γ is given by:

$$\gamma = e^{-2\pi f_u \beta T_s}$$

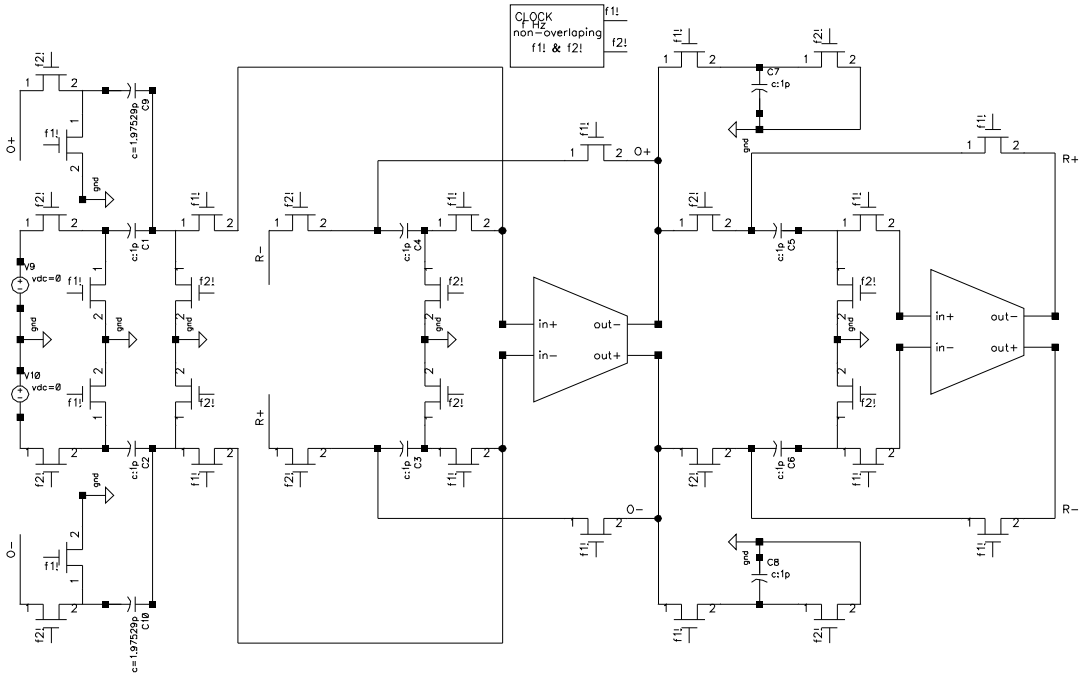

Figure 5.19: Fully differential SC implementation of a delay based resonator.

Thus, when a band-limited OTA is used in a delay based resonator loop the actual transfer function becomes:

$$H_R(z)_m = \frac{z^{-1}(1-\gamma_1)}{1+[g_1(\gamma_1-1)]z^{-1}+(\gamma_1\gamma_2-\gamma_1-\gamma_2)z^{-2}} \tag{5.31}$$

Finite f_u introduces degradation both in the Q factor of the resonator as well as in the resonant frequency. With help of *MIDAS*, the last model was simulated for different values of f_u, the results can be seen in picture 5.20. The values used for f_u were different for every OTA present in the implementation. They were taken to fix the curves in the window. As observed the required value of f_{u1} is on the order of three to 2 times bigger in order to maintain reasonable deviations of the central frequency. This is a direct consequence of the reduction experimented by β_1 in the SC implementation as discussed before. The much bigger value of the capacitor required to fix the frequency, lowering the value of β_1, would require a very high current if the displayed values of f_u should be reached. This in turn conducts to contradictory demands if a high voltage gain should be maintained in that OTA. Thus, the design of the input OTA in a delay based resonator presents a very difficult constraint.

Finally the effect of capacitor mismatch is discussed. Here, as the only parameter controlling the position of the poles of the resonator is g_1 variations in this capacitor directly translate in

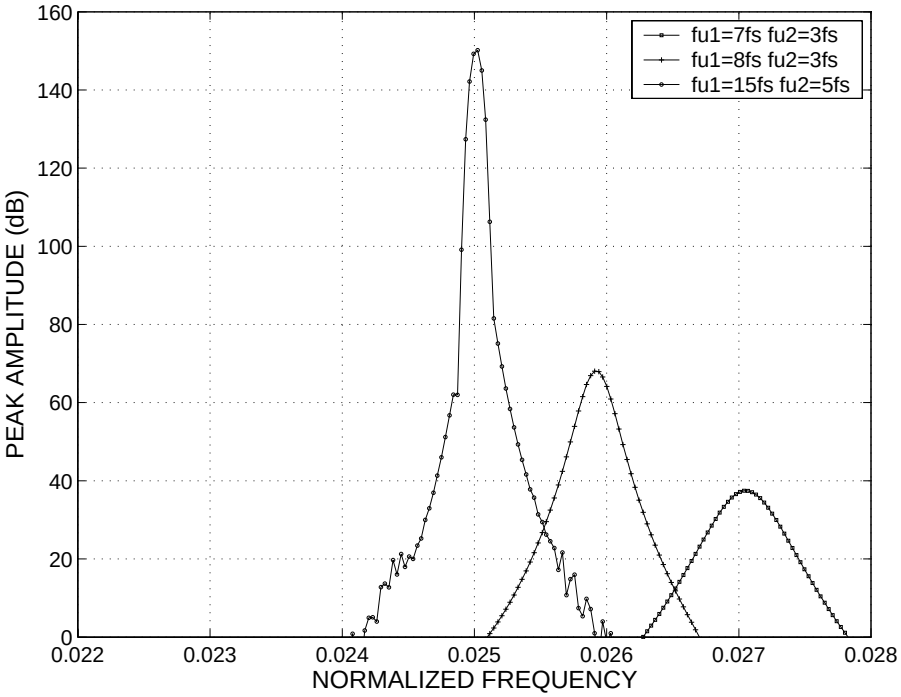

Figure 5.20: Effect of f_u in a delay based resonator.

changes of the resonant frequency. The Montecarlo simulation results for the circuit of figure 5.19 are presented in the histogram depicted in figure 5.21. From 1000 Montecarlo simulations the following results were obtained: Mean at 3.99296 MHz, standard deviation: 78.6143 kHz.

5.7 Summary

In this chapter aspects of the system level design of the proposed tri-mode ΣΔM were addressed. A discussion about the two different realization methods was presented followed by a presentation of the main architectural choices, which states as a good candidate for the implementation of a reconfigurable ADC based on the ΣΔ modulation, a high order single bit loop. With this election, the design of a NTF, that produces a stable modulator was accomplished. Previously, the method proposed by Adams et. al. to produce stable high order single bit ΣΔ loops was introduced. Using the designed NTF high-level simulations were carried out to estimate the *SQNR*, these results indicate that the required value for the maximum resolution can be reached with a low *OSR*, which is an important constraint if low power characteristics are needed. Having in mind the necessity for low *OSR*'s, the use of resonators to eliminate the quantization noise within the *BW* of interest at frequencies different than zero is demanded. SC resonators at f_s/n aimed to accomplish this noise suppression were presented and analyzed. The conducted study

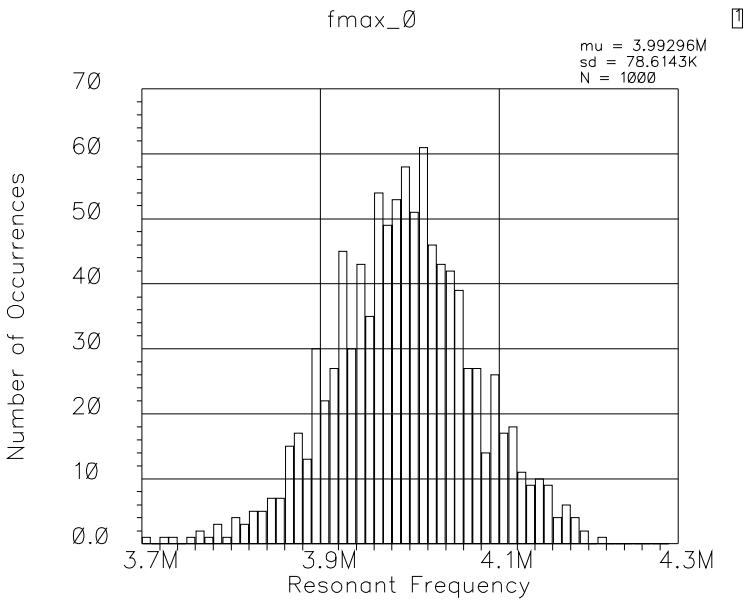

Figure 5.21: Effect of capacitor mismatch in a delay based resonator.

shows the superior performance of the integrator-based resonator over delay-based structures. As mentioned, up to the moment of writing this thesis such an analysis for SC resonators at f_s/n was not found in the literature. The sensitivity displayed by the LDI loop with respect to f_u is not very satisfactory, this gives an open field for research since digitization of wide-band signals is of great importance for up-coming communication services. The use of N-Path techniques should be reviewed for implementing resonators at frequencies f_s/n. Such techniques were not reviewed in this work because the brand new implementations showing a considerable improvement in the performance of resonators at $f_s/4$ appear during the developing of it. The next chapter addresses the synthesis of the designed NTF using the architecture of figure 5.2 and two integrator based resonators. A circuit implementation of the experimental prototype carried out in this work is also presented. The main results from the analysis of the resonant structures will be used to design the circuit elements needed in the SC implementation, and aspects of signal scaling will also be reviewed.

Chapter 6

Switched Capacitor Realization of a Tri Mode Sigma Delta Modulator

Contents

6.1 Introduction

This chapter present the SC implementation of the tri-mode ΣΔM in question. First, the synthesis of the NTF designed in the last chapter, using a cascade of elements with feed forward coefficients, will be addressed. The synthesis is finalized with the inclusion of two feedback coefficients to implement the resonators required for quantization noise suppression at frequencies different of zero. The architectural level design process described in the last chapter actually finalizes here after the signal scaling has taken place. The final architecture with scaled coefficients is presented and the stability of the design is checked by simulation after the inclusion

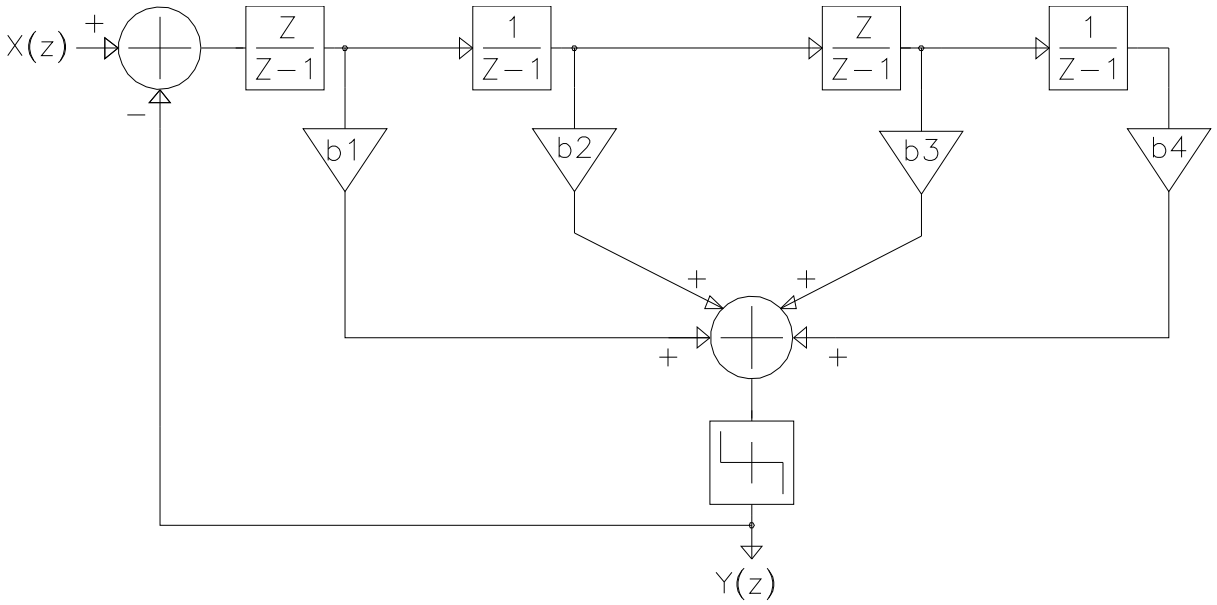

Figure 6.1: A cascade of integrators with feed forward coefficients.

of the resonator coefficients. After the final value of the coefficients is given, circuit design activities can be started. A very important element in the design of any SC system is the operational transconductance amplifier. Section 6.4 presents a review of the main OTA topologies and introduces a brief comparison of them. The elected OTA configuration is then designed for the present purposes. The single bit quantizer needed in the loop translates in a voltage comparator in the circuit implementation, section 6.5 introduces the circuit design of a regenerative comparator together with a digital output buffer. Finally, layout and floor planning of the experimental prototype are given.

6.2 Synthesis of the NTF

For our particular case, the architecture depicted in the last chapter in figure 5.2 turns in the cascade of integrators of figure 6.1, since the designed noise transfer function given in equation 5.10 and repeated here for convenience, has its four zeros at DC:

$$NTF(z) = \frac{1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4}}{1 - 3.1806z^{-1} + 3.8612z^{-2} - 2.1122z^{-3} + 0.4383z^{-4}} \tag{6.1}$$

If the quantizer of figure 6.1 is substituted by its linear model, then this architecture has a NTF given by:

$$NTF(z) = \frac{1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4}}{1 + c_1 z^{-1} + c_2 z^{-2} + c_3 z^{-3} + c_4 z^{-4}} \tag{6.2}$$

with:

$$c_1 = b_1 - 4$$

$$c_2 = 6 - 3b_1 + b_2 + b_3$$

$$c_3 = 3b_1 - 2b_2 - b_3 + b_4 - 4$$

$$c_4 = 1 + b_2 - b_1$$

To find out the values of the feed forward coefficients $b_1 \ldots b_4$ the last set of simultaneous equations must be solved equating from c_1 until c_4 to the corresponding z multiplier. Proceeding in this way, the values for $b_1 \ldots b_4$ are found to be:

$$b_1 = 0.8194$$

$$b_2 = 0.2577$$

$$b_3 = 0.0617$$

$$b_4 = 0.0067$$

In order to implement the resonators, required to move the zeros of the NTF away form DC, coefficients g_1 and g_2 must be added as shown in figure 6.2. As discussed, these two resonators are needed to maintain a low OSR in wide-band applications, since these coefficients will be disconnected for narrow band signals. The presence of g_1 and g_2 in the architecture modify the numerator of equation 6.2 to:

$$1 + z^{-1}(g_1 + g_2 - 4) + z^{-2}(6 - 2(g_1 + g_2)) + z^{-3}(g_1 + g_2 - 4) + z^{-4} \tag{6.3}$$

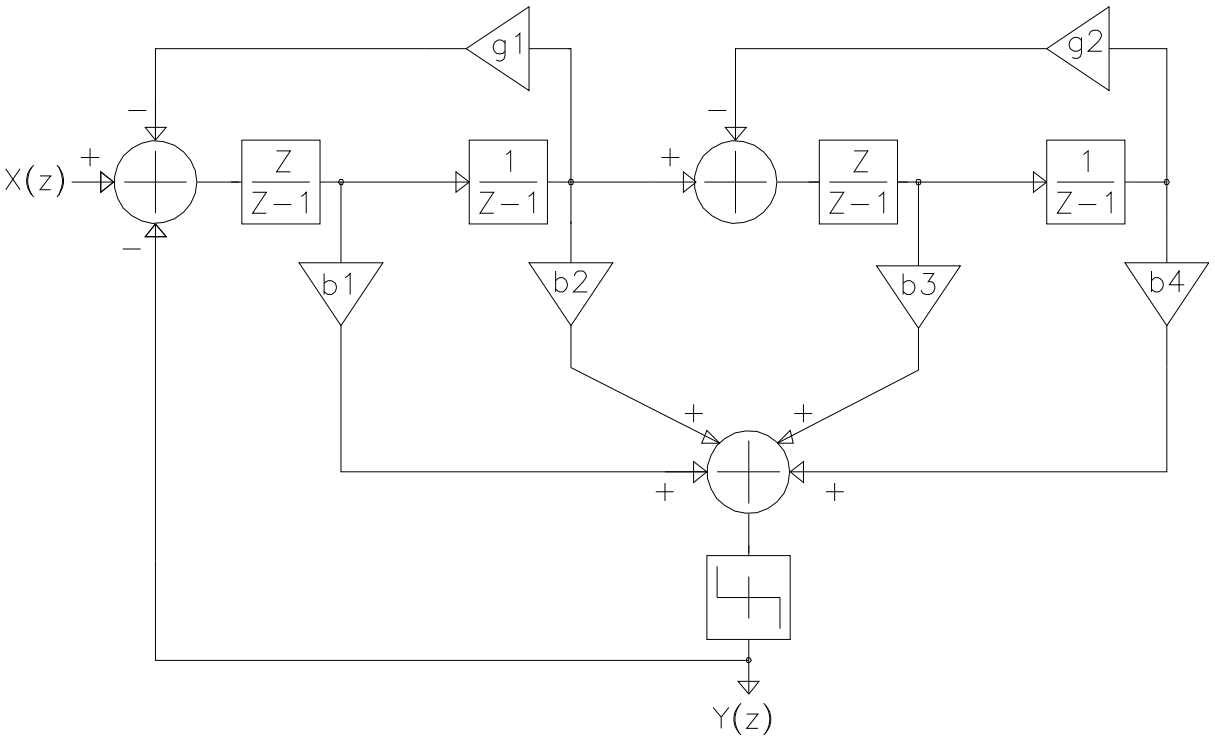

Figure 6.2: A cascade of integrators with two local resonator coefficients.

In [47] the optimal NTF zero positions for a fourth order modulator are given as pairs of complex conjugated numbers:

$$zero_1 = 0.9986 \pm 0.0534\,j$$

$$zero_2 = 0.9909 \pm 0.1349\,j$$

using this values with equation 5.18 produces the following values for the resonator coefficients:

$$g_1 = 0.0029$$

$$g_2 = 0.0183$$

Using this set of coefficients, the spectrum of the output signal produced by the architecture of figure 6.2 was found through simulations. The estimation of the FFT was repeated twice in

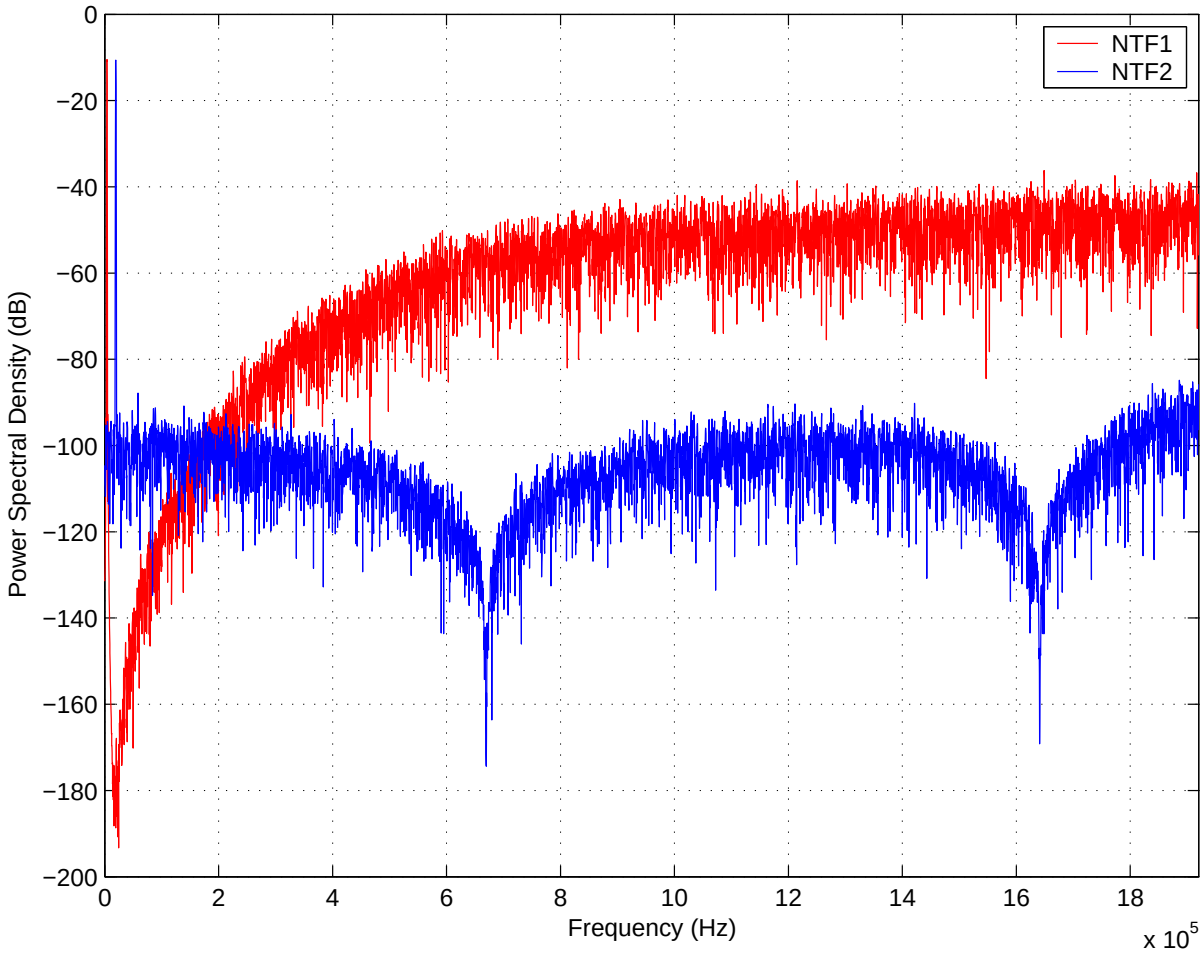

Figure 6.3: Output spectrum from fig. 6.2 for narrow- and wide- band signals

order to observe the effect of the resonators. The results presented in figure 6.3 show the power spectral density for the first NTF (Eq. 6.1) with a CLK frequency of 16 MHz, which produces an OSR of 40 for GSM signals and with $f_{CLK} = 76.8$ MHz equivalent to $OSR = 20$ for $BW/2$ of UMTS signals if the factors g_1 and g_2 are included to modify the numerator of eq. 6.1 to that written in eq. 6.3. From figure 6.3, the effect of g_1 and g_2 is clear.

6.3 Operational Transconductance Amplifier (OTA) Design

6.3.1 Candidate OTA Topologies

Operational transconductance amplifiers, characterized by the absence of an output buffer and having so a high output resistance, are the ones preferred for SC implementations. In princi-

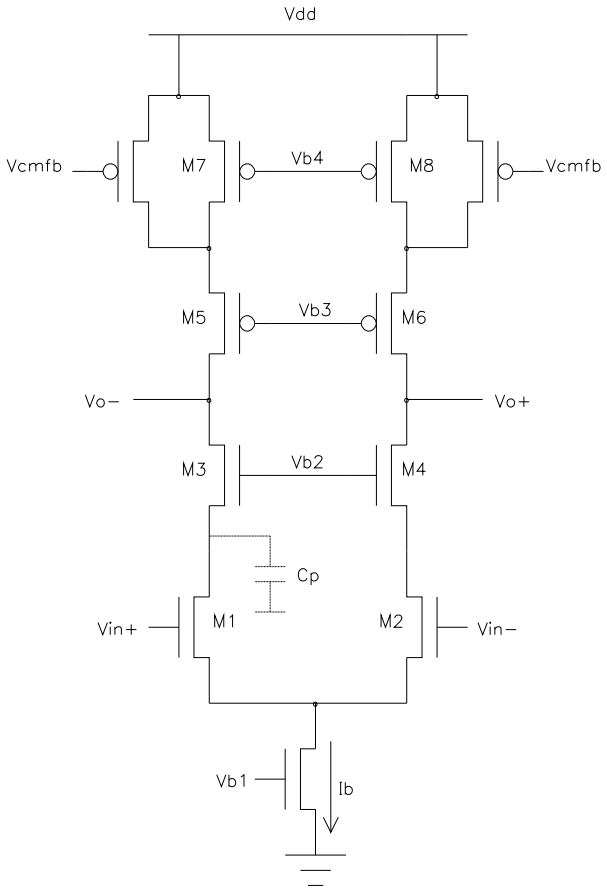

Figure 6.4: Fully differential telescopic cascode OTA.

ple, in a SC network the op. amps. are embedded in an environment, in which they do not experiment resistive loads, only a purely capacitive load, thus, the output resistance presented by the amplifier is not a design constraint. There are mainly three OTA architectures found in the literature, namely, the *telescopic cascode*, *folded cascode*, and the *two stages* or *Miller compensated* OTA. Due to their importance, they have been extensively analyzed in textbooks [54, 55] as well as in doctoral investigations [56]. There are also refinements to improve certain characteristics such as output signal swing or voltage gain of single stage architectures. This last topic has covered great attention, because of the aggressive scaling of CMOS technologies in the last years and a useful method to enhance the voltage gain has evolved in the so-called *gain boosting technique*, [57, 58], of which, a detailed analysis and design methodology is found in [59]. Here, our objective is to present a brief review and comparison of the main characteristics of each fundamental topology in order to introduce the elected op. amp.

Telescopic Cascode:

The basic implementation of a fully differential telescopic cascode OTA is presented in figure 6.4. The simple construction of this op. amp. reflects the benefits of a single stage ampli-

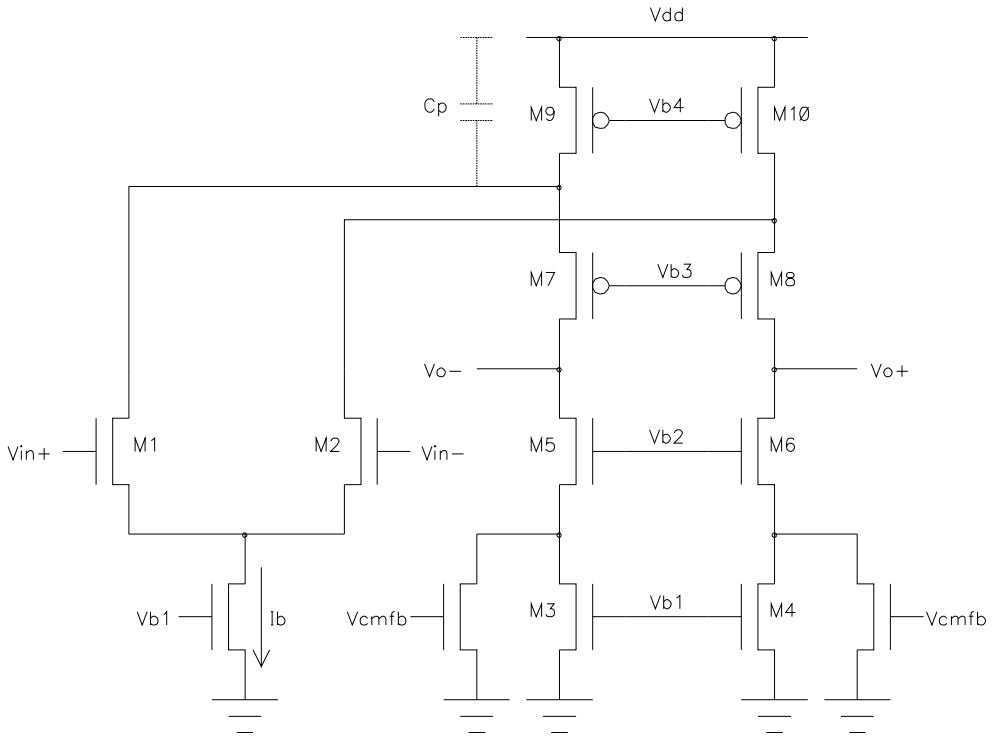

Figure 6.5: Fully differential folded cascode OTA.

fier, namely low power consumption and high frequency response. It posses the highest non-dominant second pole defined by the transconductance of the cascode transistors M3 and M4 as well as the parasitic capacitances at the drains of the input differential pair M1 and M2. The voltage gain of this OTA is equal to the transconductance (g_m) of the input devices multiplied by the load resistance. This value of g_m, together with the load capacitance C_L, defines the unity gain frequency (f_u) of the amplifier. The main disadvantage of the telescopic cascode OTA is its reduced output signal swing, which is limited to $Vdd - 5Vds_{sat}$, which makes it inadequate for low voltage supply under 3V. Furthermore, the input common mode level has to be set quite accurately and the allocated margin further reduces the output voltage range. However, the usage of a wide swing current mirror in the cascode load [54] joined with signal scaling can help to alleviate these problems to a certain degree.

Folded Cascode:

A folded cascode OTA is depicted in figure 6.5. The output node of this amplifier has 4 stacked devices between Vdd and ground, making the output signal swing of this circuit somewhat larger than that of the telescopic cascode. In this case, the output range is extended to $Vdd - 4Vds_{sat}$. Although this represents an improvement in this characteristic, it is accomplished at expenses of doubling the power consumption because of the added output paths. The unity gain frequency of this amplifier is defined in the same way as for the telescopic cascode,

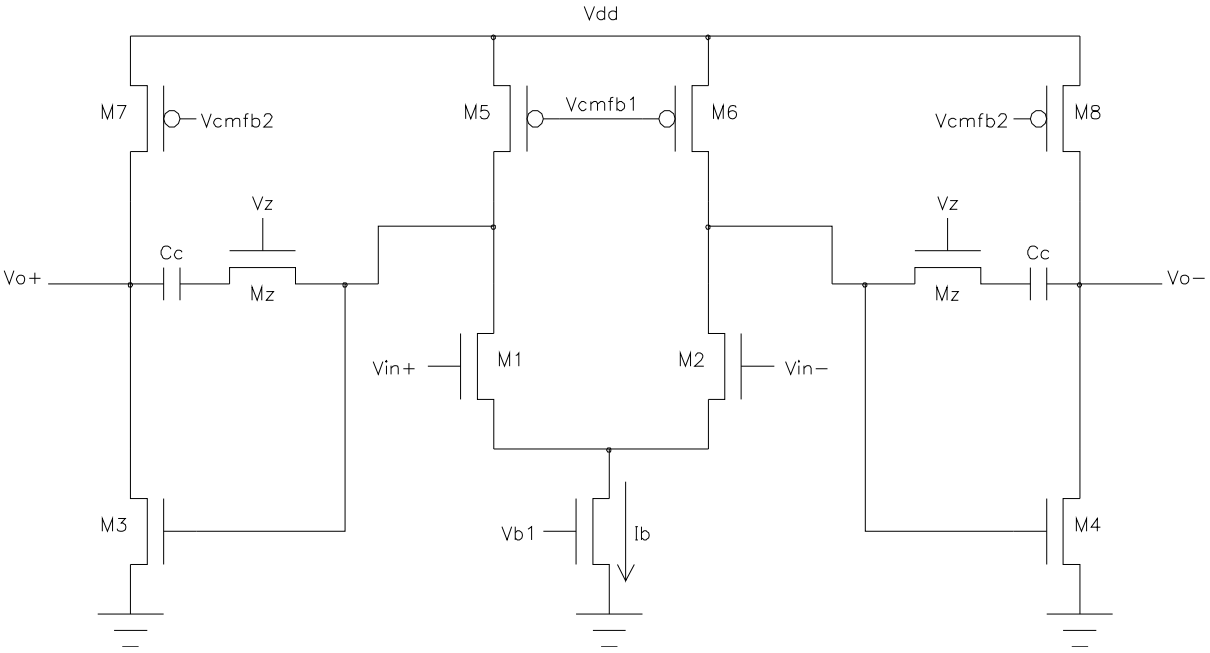

Figure 6.6: Fully differential two stages OTA.

however, the second pole of this circuit is located at lower frequencies because it is defined by the transconductance of PMOS devices M9 and M10 and the capacitance seen from the drain of these devices to ground. This in turn lowers the phase margin (PM) and reduces the allowed f_u for a given PM. The most attractive characteristic of this OTA is the possibility of electing the input and output common mode range separately, as well as the larger value of these intervals.

two stages OTA

Figure 6.6 shows a fully differential implementation of a two stages OTA. In contrast to the previous topologies, this OTA achieves its voltage gain using a differential pair in cascade with a common source amplifier. Stable operation of this circuit in negative feedback loops requires the usage of internal compensation achieved by the capacitors Cc and mosfets Mz. This capacitor defines in turn the amplifier f_u. This compensation usually leads to a sacrifice in the gain-bandwidth product as compared with single stage amplifiers. As shown in picture 6.6, the fully differential implementation of this OTA requires two common mode feedback circuits in order to control each stage. The main advantage of this classical topology is the improved output signal swing with respect to that of the cascoded amplifiers, which makes this circuit a good candidate for designs with low power supply below 2.5V, where the use of cascoded devices is unfeasible.

We close this discussion with a resume of the OTA characteristics presented in table 6.1, where the noise performance of each architecture is included, and as we can see, the folded cascode topology has the worst noise behavior.

	Telescopic Cascode	Folded Cascode	Two Stages
A_V	$\frac{g_{m1}}{\frac{g_{ds7}g_{ds5}}{gm_5}+\frac{g_{ds3}g_{ds1}}{gm_3}}$	$\frac{g_{m1}}{\frac{g_{ds3}g_{ds5}}{gm_5}+\frac{g_{ds7}(g_{ds2}+g_{ds9})}{g_{m7}}}$	$\frac{g_{m1}}{g_{ds1}+g_{ds5}}\frac{g_{m3}}{g_{ds7}+g_{ds3}}$
f_u	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_L}$	$\frac{g_{m1}}{C_C}$
SR	$\frac{I_b}{C_L}$	$\frac{I_b}{C_L}$	$\frac{I_b}{C_C}$
I_{Vdd}	I_b	$2I_b$	$3I_b$
Output Swing	$Vdd-5Vds_{sat}$	$Vdd-4Vds_{sat}$	$Vdd-2Vds_{sat}$
Second Pole position	$\frac{g_{m3}}{C_p}$	$\frac{g_{m7}}{C_p}$	$\frac{g_{m3}}{C_L}$
Noise	$\frac{8kT}{g_{m1}}\left(\gamma_1+\gamma_7\frac{g_{m7}}{g_{m1}}\right)$	$\frac{8kT}{g_{m1}}\left(\gamma_1+\gamma_3\frac{g_{m3}}{g_{m1}}+\gamma_9\frac{g_{m9}}{g_{m1}}\right)$	$\frac{8kT}{g_{m1}}\left(\gamma_1+\gamma_5\frac{g_{m5}}{g_{m1}}\right)$

Table 6.1: Comparison of basic OTA topologies

b_1	b_2	b_3	b_4	c_1	c_2	c_3	c_4	g_1	g_2
5.4626	3.0070	2.0567	2.1613	0.1500	0.5713	0.3500	0.1033	-0.0315	-0.0290

Table 6.2: Scaled coefficients of the modulator

The excellent frequency behavior and low power consumption of the telescopic cascode OTA are the reasons behind its election as active element in the implementation of the experimental prototype. As shown in the last chapter, in section 5.6.3, a f_u of around four times f_s is needed in the OTA, if the Q factor of the resonator has to be maintained in an acceptable level. This constraint makes the frequency response of the op. amp. an important parameter to be considered in the election of the amplifier to be used in the implementation. The problem depicted by the telescopic cascode, concerning its limited output signal swing, can be partially solved by the remaining signal scaling step of the design methodology described in the last chapter. Taking into account the large f_u requirements, we decided to use an overdrive voltage $(V_{gs}-V_T)=0.5$ this produces a value of 500 mV for Vds_{sat} in each device of the amplifier. According with the values given in table 6.1 and with the maximum power supply $Vdd=3.3$ V of the available technology, we get a voltage swing of 0.8 V, which corresponds to a 24.24% of the total available voltage range for signal swing. We choose a factor of 0.33 in order to accomplish signal scaling, according to the method described in [40], since the differential swing of the op. amps is 48.48%. The scaling process asks for the inclusion of coefficients $c_1 \ldots c_4$ in the modulator architecture, as shown in figure 6.7. After scaling, the final values of the coefficients are given in table 6.2.

As it can be concluded form the values of the final coefficient set, the scaling procedure, i.e. reducing the signal levels at the output of the integrators typically increases the load of the amplifier, and for that reason these structures are not suitable for low voltage. This fact should also motivate research in the developing of new resonator architectures a f_s/n aimed for wideband digitization at baseband and adequate for the low power supply of the current and future

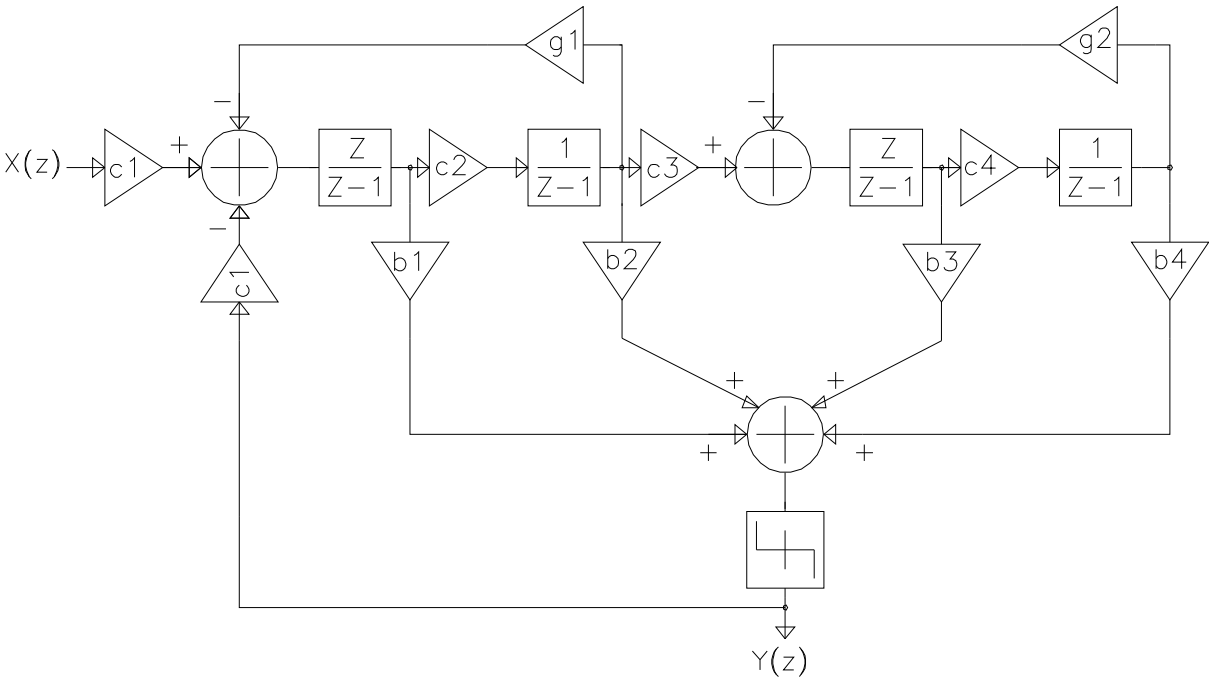

Figure 6.7: Cascade of resonators with feedforward and scaled coefficients.

technologies. At this point, as we have finished our architectural design and have taken and operational amplifier topology we are ready to start circuit design.

6.3.2 Behavioral analysis and OTA specifications

This section presents the simulation results from behavioral simulations perfomed with *MIDAS* in order to obtain the specifications for the design of the operational amplifiers. As performance parameter the *signal-to-noise and distortion ratio* $(SNDR)$ was taken. The inclusion of distortion is important here because some of the circuit non-idealities such as slew rate degrade the modulator's performance rather by distortion of the input signal than increase of the inband noise floor. A sinusoidal input at 2.533 kHz and 12.1565 kHz for narrow- and wide- band signals was taken respectively. The input signal level was put at -4 dB under the quantization levels, as this is the point of maximum *SNR*. The non-ideal effects analyzed were finite A_V, f_u and slew rate (SR).

Effect of finite OTA DC-Gain

As the model of equation 5.23 shows, finite voltage gain introduces, both gain and pole position error in a SC integrator. The effect is also influenced by the feedback parameter β. As β is exactly known having the SC implementation of the modulator with all required capacitor ratios, we choose for the simulations a pessimistic value of 0.4 for beta, although an inspection to the

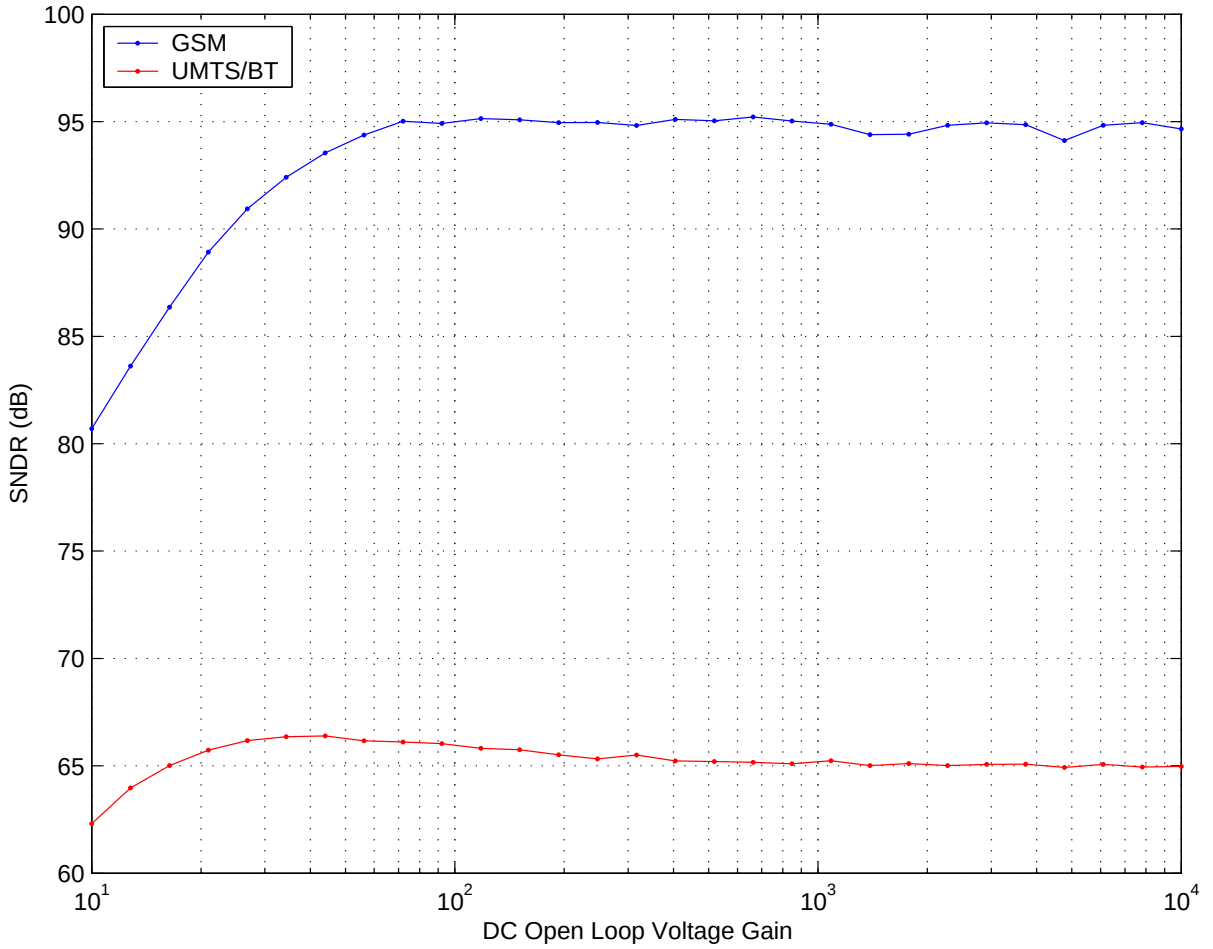

Figure 6.8: *SNDR* performance versus OTA DC gain.

coefficient set of table 6.2 indicates that the value of the feedback factor will be always bigger than 0.5, since coefficients c_n all have a value smaller than 1. The model of eq. 5.23 neglects some effects like the non-linearity of the voltage gain as a function of the output voltage and the effect of the non-zero on-resistance of the switches present in the implementation, which would modify the equivalent circuit of figure 5.12 used in the developing of the model. For these reasons, the very optimistic values presented in figure 6.8 should be taken with reserve and values of A_V close to 60 dB should be used. At 60 dB or above this value of A_V, the charge transfer errors are determined by the deviation of the capacitor ratios from their nominal values, rather than the charge loss due to finite voltage gain.

Effect of finite unity-gain frequency

Finite f_u introduces in an integrator only a gain error, as stated in equation 5.25. However this error manifests as both gain and pole deviation when a bandwidth-limited integrator is embedded in a LDI loop, as given in the model 5.26. The effect of finite f_u is especially severe

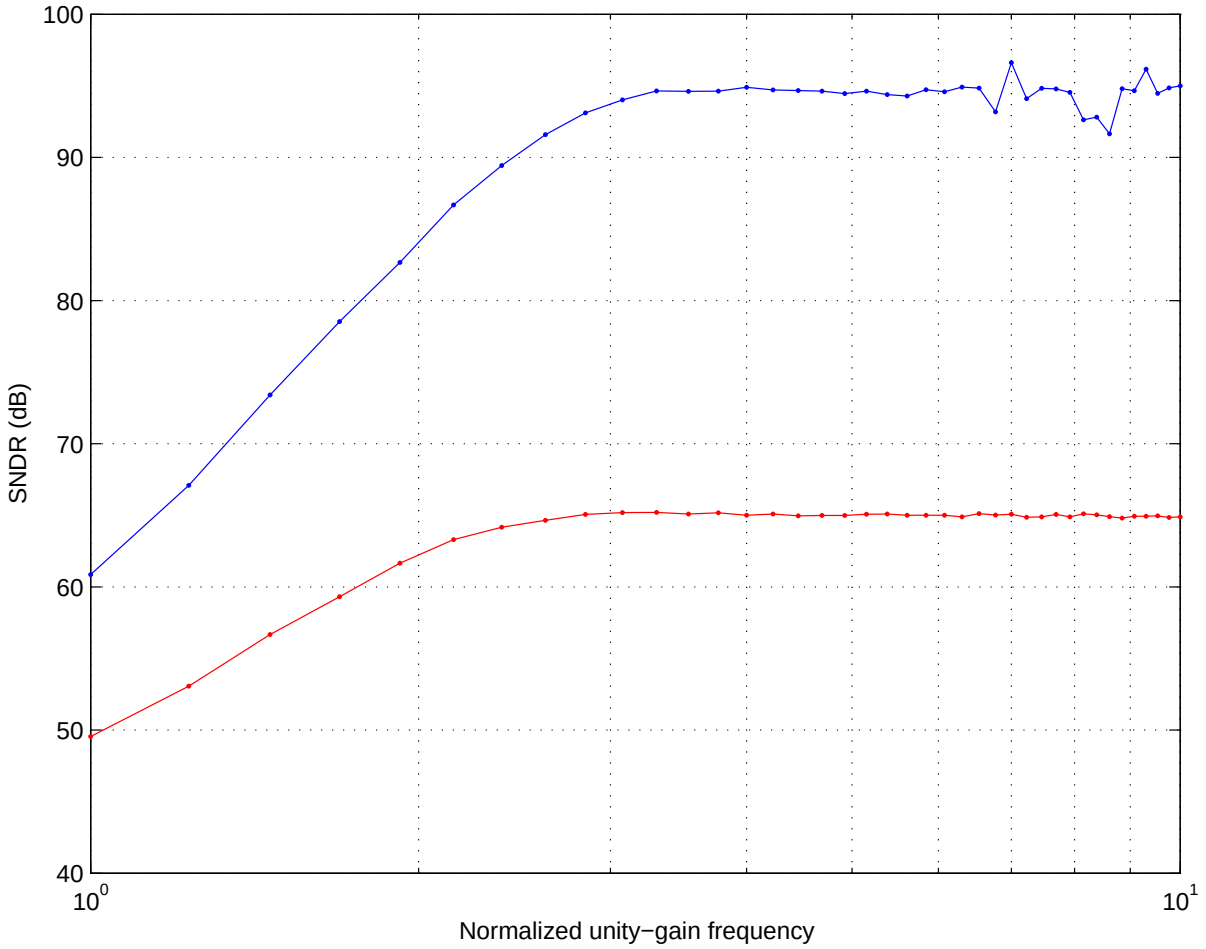

Figure 6.9: *SNDR* performance versus OTA f_u.

with respect to the Q factor of the resonator, as we have seen in the results displayed in figure 5.15. The integrators used in the modulator were modeled with eq. 5.25 in order to perform the high level simulations. This model neglects also the on resistance of the switches and assumes that, the OTA has infinite A_V and the second pole is located well above f_u, this restriction asks for the use of very well compensated OTA's in the implementation. The results of the high level simulations carried out including the gain error produced by finite f_u are shown in figure 6.9. The x axis of figure 6.9 presents the values of f_u normalized to f_s. It can be seen that the high-resolution mode of operation needs, for an optimum performance, a $f_u > 3.25\,f_s$ while for wide band signals $f_u > 3\,f_s$ must be obeyed. This produces minimum values for f_u of 52 MHz and 230.4 MHz for GSM and UMTS signals respectively.

Effect of finite Slew Rate

The most destructive effect in the performance of the modulator is due to finite output slew rate. *SR* determines the time available to the integrator for exponential settling after slewing. If *SR*

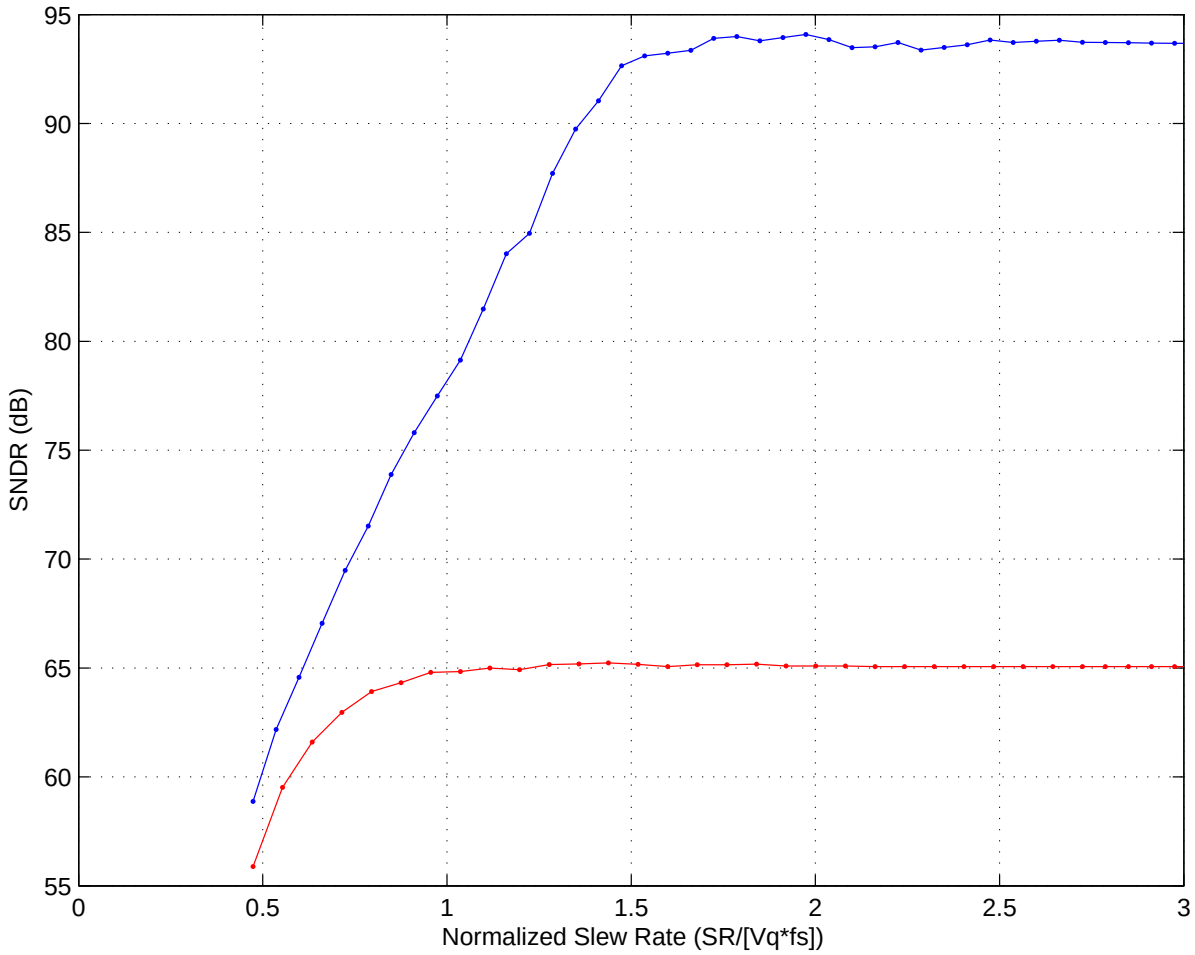

Figure 6.10: *SNDR* performance versus OTA *SR*.

is low, this time decreases and large settling error occurs. In the limit, only slewing takes place during the available settling time. Such a situation can leave the modulator in an unstable condition. For proper operation of the system, the maximum slewing interval has to be kept within an appropriate fraction of the available settling time. Figure 6.10 illustrates the *SNDR* performance versus slew rate while the f_u was kept constant at $3f_s$ for both modes of operation. The slew rate is normalized to the product of quantization voltage (V_q) and clock frequency f_s. The high-resolution mode of operation requires normalized slew rate greater than 1.5. Otherwise a sharp *SNDR* decrease is experimented, which produces a slew rate requirement of 79.2 $V/\mu s$ for the available technology with power supply voltage of 3.3 V. The low resolution- wideband-mode needs for proper operation a normalized *SR* bigger than 1, this means 253.44 $V/\mu s$ at least.

The information collected from these results is summarized in table 6.3. The requirements displayed in that table should be taken as estimations to have a basis for the circuit design and

	A_V (dB)	f_u (MHz)	SR (Vμs)
GSM	60	52	79.2
BT	60	60	66
UMTS	60	230.4	253.44

Table 6.3: Estimated OTA requirements

not as definitive values, due to the already mentioned limitations of the models. The neglected effects were taken according to their importance and to keep the equations tractable.

6.3.3 Capacitor sizing

As discussed in the last chapter in section 5.5, the size of the sampling capacitor in a sample and hold circuit is determined by the so called kT/C noise. Equation 5.9, which states the capacitor value for certain number of bits, is repeated here for convenience:

$$C \approx \frac{kT \times 12}{2^{-2N} V_{REF}^2}$$

This relation produces capacitor values of 1.22 pF for 14 bits of resolution and a full-scale voltage $V_{REF} = 3.3$V. The nature of the kT/C noise is thermal and uniformly distributed from DC to $f_s/2$. The value required by the high-resolution mode of operation is fairly big and would produce a very large total capacitive load for the OTA's. As the modulator will work with an $OSR = 40$, the properties of the thermal sampling noise enable us to reduce the capacitor by this factor, since the noise power will be uniformly distributed from DC to $f_s/2$. The linear reduction by 40 produces a capacitor of 30.5 fF. If this capacitor size is taken as input capacitor in the first integrator, according to the values of the scaled coefficients, an integrating capacitor of 203.33 fF would be needed and the capacitor implementing g_1 would be equal to 6.4 fF. Both the sampling and the g_1 capacitor exhibit small values that would compromise the matching of them after fabrication. Especially the value of the capacitance needed for g_1 results very small, such a capacitance value would be strongly influenced by the parasitics associated to its nodes and would result in changes in the pole position of its associated resonator.

As a compromise between capacitor matching, silicon area and OTA load, a sampling capacitor at the input with a value of 150 fF was chosen. This coincidently produces an integrating capacitor of 1 pF for each stage of the modulator. The implemented SC network with the final capacitor values is shown in figure 6.11.

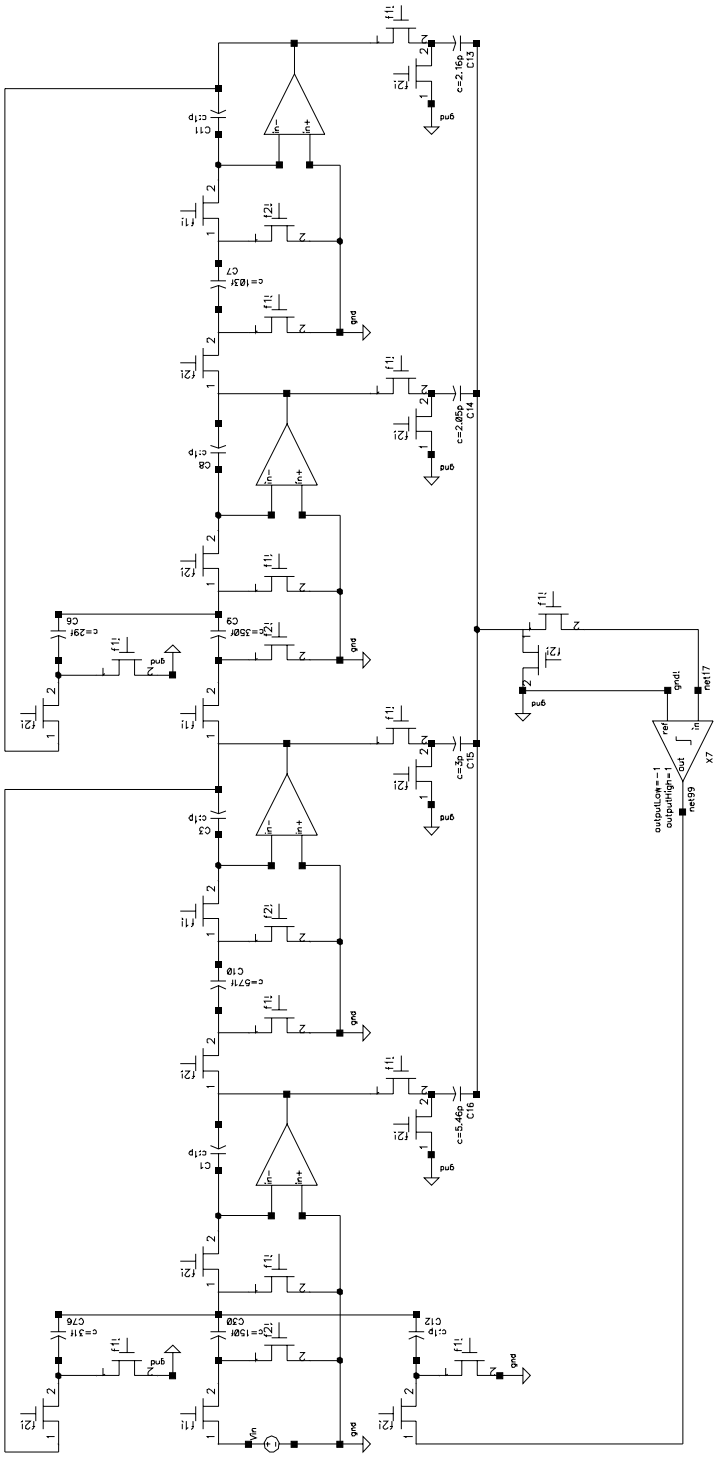

Figure 6.11: Single ended circuit diagram of a 4th. order ΣΔM.

	OTA 1	OTA 2	OTA 3	OTA 4
C_L (pF)	6.28	2.86	2.43	1.8

Table 6.4: Capacitive load of each OTA

The clock distribution used is such that every integrator adds a half delay to the signal, while the output of each OTA is being sampled in the integration phase, as shown in the figure 6.12, which represents the first integrator of the modulator. Although this clock distribution augments the load seen by the amplifiers in comparison with the clock distribution used in [3], the schema adopted here leaves the design open to add another network of switches and capacitors controlled by the opposite phases, so implementing a double sampled modulator as in [51], which should improve the speed performance of the present design by a factor two without incrementing the power consumption. With this clock distribution, the capacitive load experimented by each OTA is depicted in figure 6.13 when the coefficients g_1 and g_2 are active, as is the case for UMTS signals. The values of the equivalent load are written in table 6.4. With this information and the requirements estimated by the high level simulations, the necessary amplifiers were designed. The maximum rates of *SR* and f_u required by the signals of the UMTS standard were used as design constraints. The moderate values of unity gain frequency and slew rate needed by the BT and GSM standards could be obtained by adjusting the bias current i_b of each operational amplifier to the desired values. This would be implemented by an external current source used to generate i_b in a variable fashion, as illustrated in figure 6.14

The final dimensions of the transistors comprised by each OTA, as well as their characteristics obtained by simulation are summarized in table 6.5. The election of the telescopic cascode OTA represents a good option, since the requirements imposed to the amplifiers require a moderate voltage gain and high speed. Also, having in mind the flexibility required by the converter, the main parameters of the OTA can be controlled by the current i_b in an accurate way.

In order to select the operating mode, the capacitors implementing the coefficients g_1 and g_2 must be connected for wide-band signals and disconnected for digitisation of narrow-band signals. This is going to be accomplished by the selection logic shown in figure 6.15. Here, an external control signal with a logic value of 1 should leave the coefficient active, while a logic value of zero disables the resonator feedback by connecting both plates of the capacitor to ground.

6.4 Comparator and Output Buffer

The one bit quantizer of figure 6.7 is implemented using a fast regenerative comparator with pre-amplification [60] and a master/slave RS flip-flop. Two amplification stages were needed

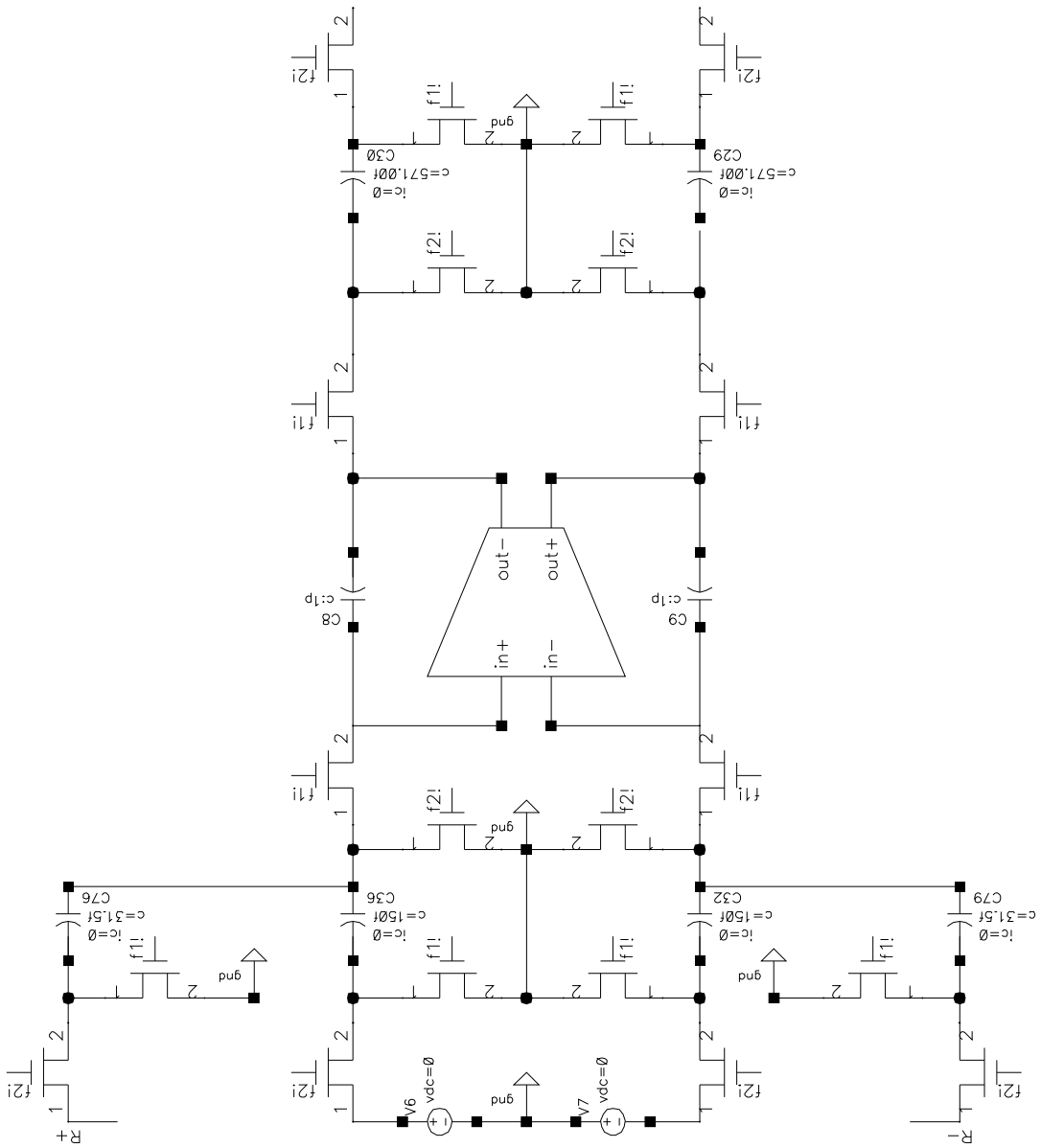

Figure 6.12: Switching schema used in the proposed ΣΔM.

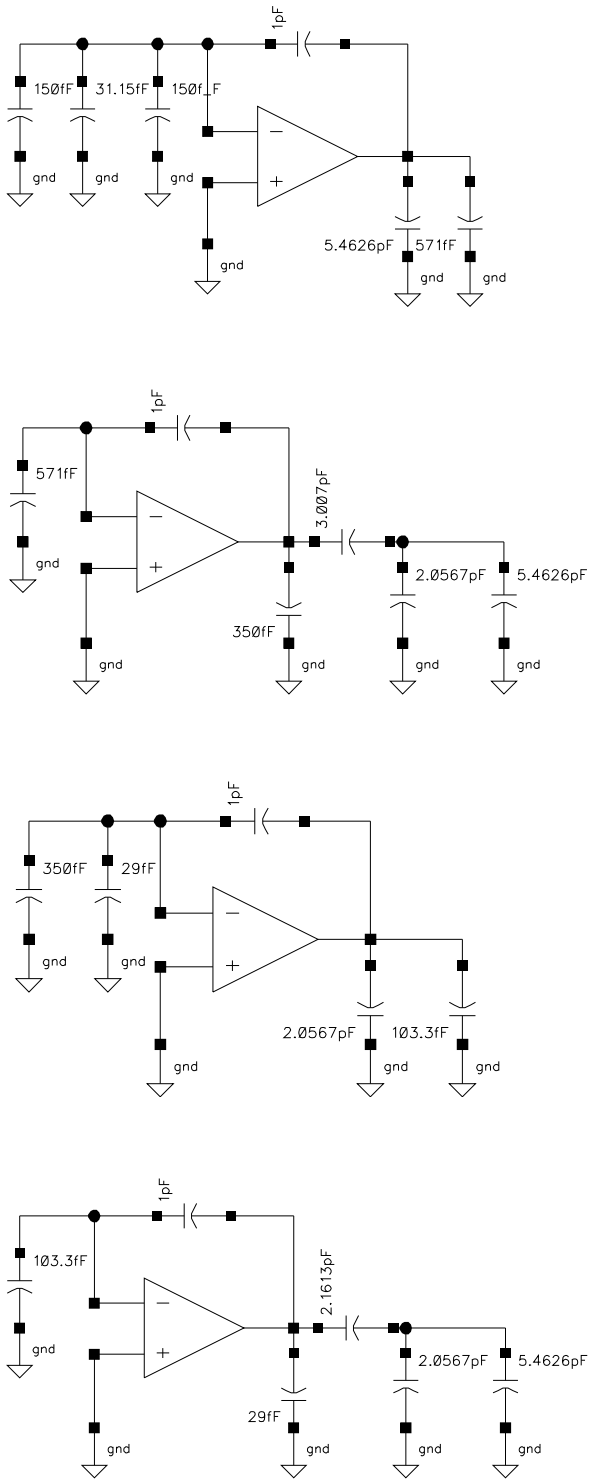

Figure 6.13: Capacitive load of each OTA.

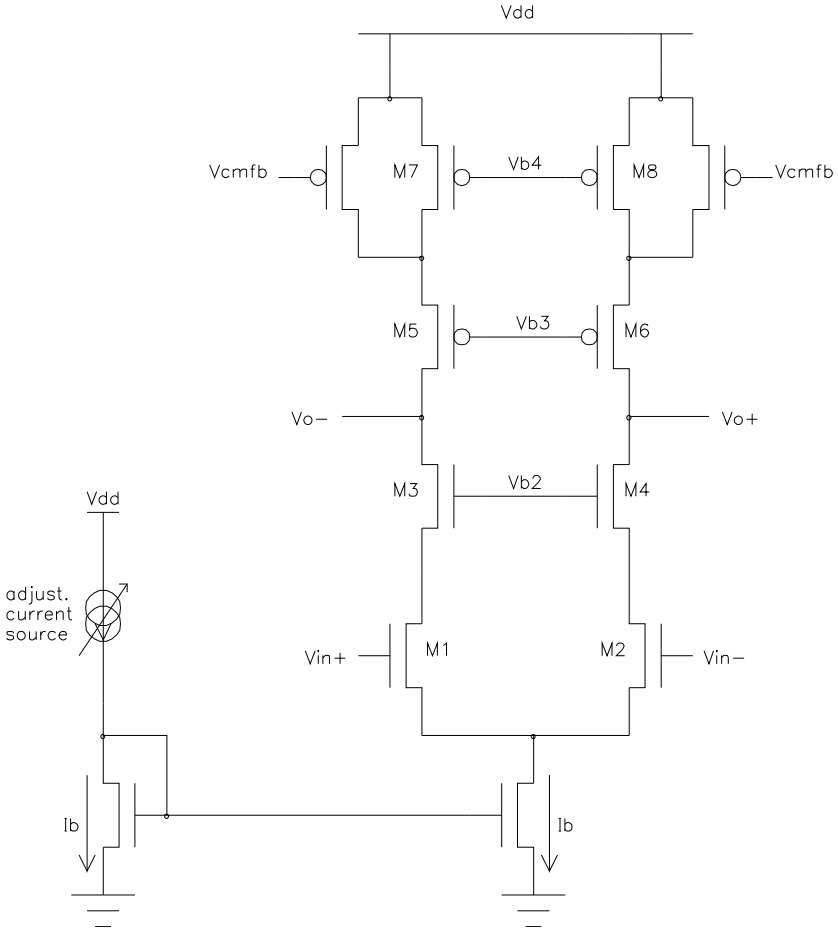

Figure 6.14: Use of a variable current source to adjust *SR* and f_u.

	OTA 1	OTA 2	OTA 3	OTA 4
i_b (mA)	5	2.28	2.95	1.44
$\frac{W}{L}$ 5,6,7,8 (μm)	$\frac{997}{1.5}$	$\frac{454.3}{1.5}$	$\frac{387}{1.5}$	$\frac{285.7}{1.5}$
$\frac{W}{L}$ 3,4 (μm)	$\frac{324.7}{2}$	$\frac{148}{2}$	$\frac{126}{2}$	$\frac{93}{2}$
$\frac{W}{L}$ 1,2 (μm)	$\frac{48,8}{0,3}$	$\frac{22,2}{0,3}$	$\frac{18,9}{0,3}$	$\frac{13,9}{0,3}$
$\frac{W}{L}$ ib (μm)	$\frac{649.4}{2}$	$\frac{296}{2}$	$\frac{252}{2}$	$\frac{186}{2}$
$\frac{W}{L}$ cmfb (μm)	$\frac{498.6}{1.5}$	$\frac{227}{1.5}$	$\frac{193.4}{1.5}$	$\frac{142.8}{1.5}$
A_V (dB)	57	57	57	57
f_u (MHz, $C_L = 1$pF)	256	225	174	145
SR (V/μs)	581	571	635	562
PM (degree)	71	76	77	79

Table 6.5: Transistor sizes and OTA paremeters

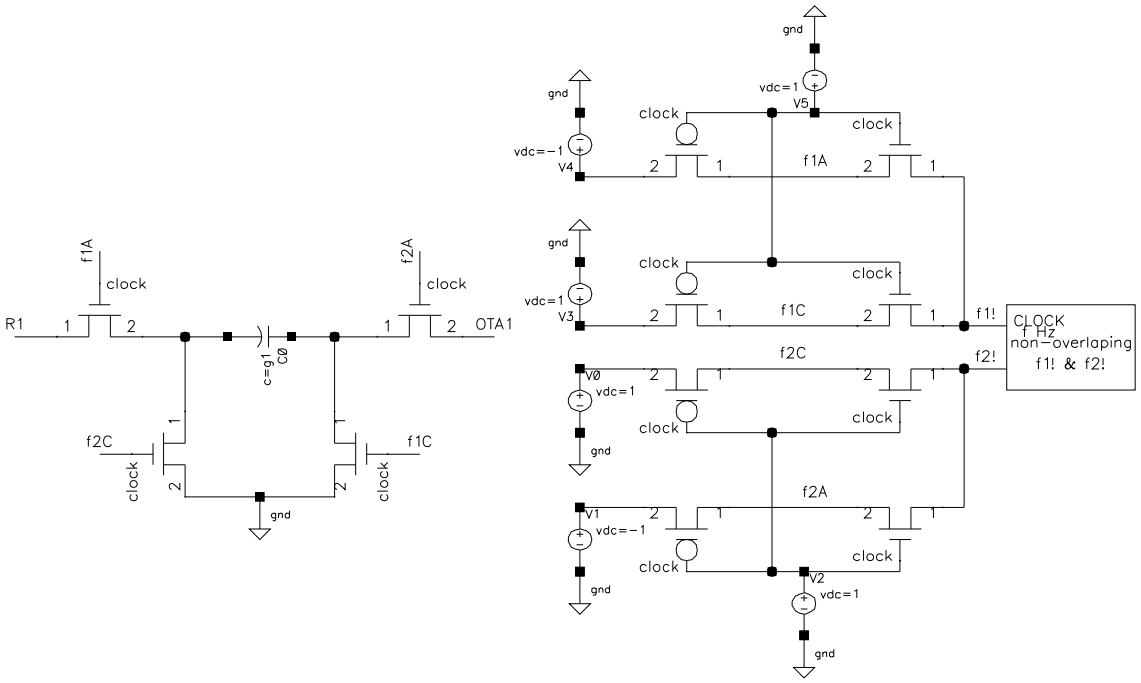

Figure 6.15: Selection mode circuit.

because the internal states scaling reduces the signal swing at input of the comparator. Circuit level simulations revealed a considerable degradation of the spectrum of the output signal, if a single stage comparator were used. The regenerative comparator employed here is depicted in figure 6.16. The final sizes of the transistors are written in table 6.6.

The master/slave RS flip-flop is controlled by the positive edge of $f1!$ and holds the data for a full clock cycle. This memory element is illustrated in figure 6.17. In order to drive the large capacitive load of the output pad, the Q terminals of the flip-flop are followed by an output buffer, this buffer is composed by 4 logic inverters connected in cascade as displayed in the same figure and was designed to drive a load capacitance of around 2.7nF at a clock frequency of 160 MHz. All transistors comprised by the output buffer are using minimum channel length $(0.3\mu m)$. The width of every transistor in the buffer from the first to the fourth inverter is 16.5μm, 44.7μm, 121.2μm and 326.4μm for the P transistors and 5.5μm, 14.9μm, 40.4μm and 109.5μm for the N transistors.

The common mode feedback circuit used to control the output common voltage of the OTAs was a SC circuit. Both the input common mode and output common mode voltage was chosen to be half of the power supply (1.65) in order to have maximum signal swing. All switches in the modulator were implemented using parallel connected P and N mosfets with minimum channel length and an aspect ratio equal to 100 and 33 respectively. The common mode feedback circuit is depicted in figure 6.18.

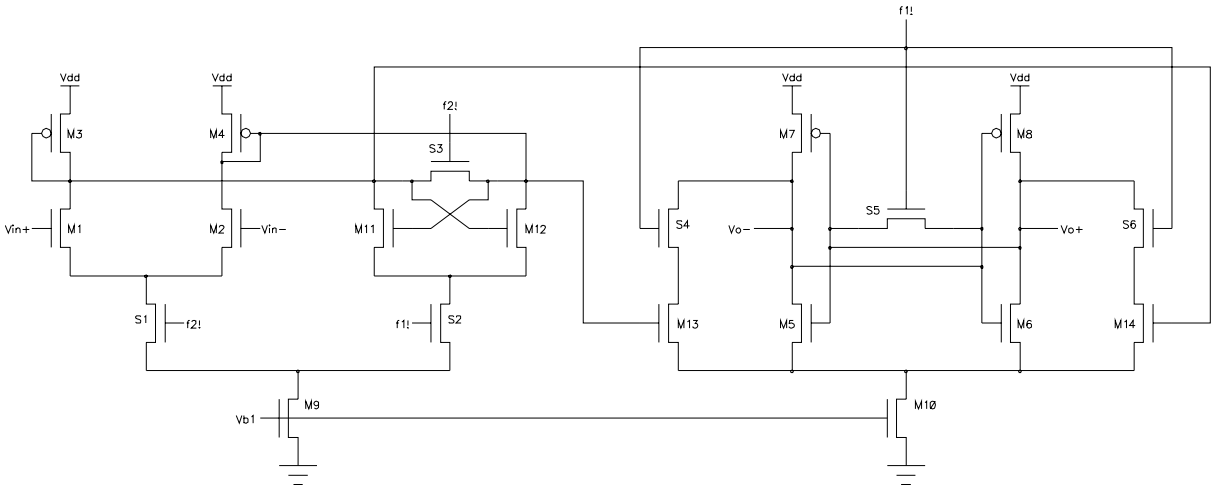

Figure 6.16: The used regenerative comparator.

Transistor	W (μm)	L (μm)
$M_{3,4}$	40	2
$M_{7,8}$	9.2	0.5
$M_{1,2}$	15	0.3
$M_{s1...s6}$	4.1	0.3
$M_{11,12}$	2	0.3
$M_{13,14}$	12	0.3
$M_{5,6}$	5	0.3
M_9	20	1
M_{10}	28	1

Table 6.6: Transistor sizes of the comparator

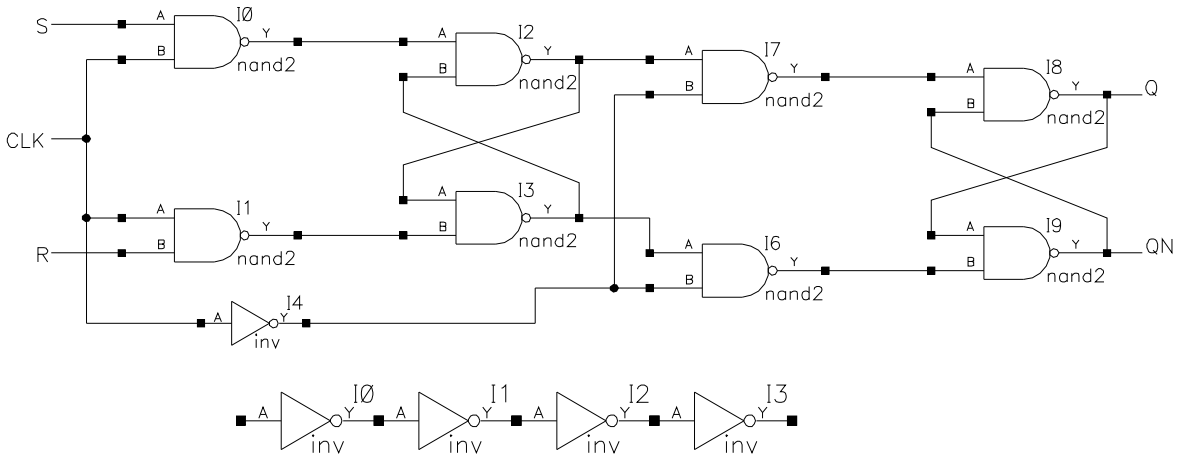

Figure 6.17: Flip-flop and output buffer.

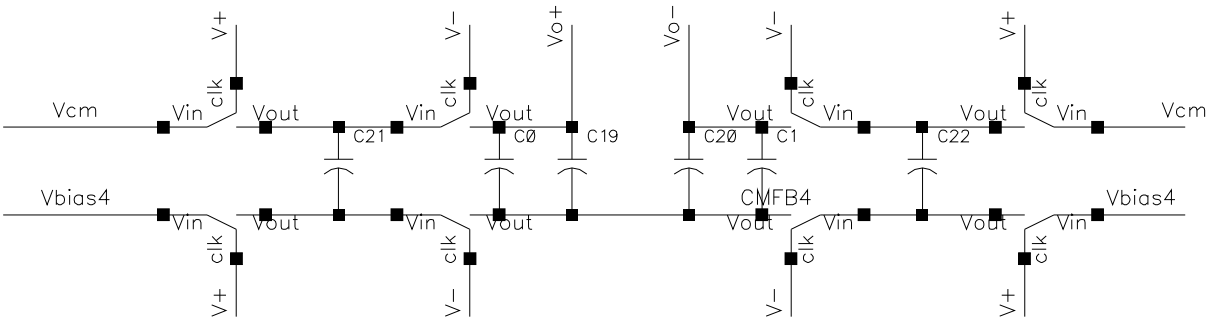

Figure 6.18: SC common mode feedback circuit.

6.5 Floor Planning and Layout Design

In the experimental prototype, the analog floor plan was carried out following the recommendations given in [61]. Special care was taken in using common centroided elements to build the input differential pairs of the four OTAs. Dummy elements were extensively used in order to improve the matching of the capacitors. Where it was possible, the large value capacitors were constructed by parallel connection of a unit capacitor of 150f F, and where not, it was tried to keep the same capacitor area/perimeter ratio. In some cases none of the mentioned matching techniques were able to be applied because of the widespread coefficient values. In such cases, care was taken to have those capacitors surrounded by dummy elements. The floor plan can be found in figure 6.19, where a die micro photograph of the fabricated design is shown. There, the distribution of the components is marked. Separated pads were used for analog and digital V_{dd} as well as for ground. Both analog and digital ground were externally connected in order to prevent latch-up. The total amount of silicon area comprises 1 square milimeter.

6.6 Summary

In this chapter, the main aspects of the circuit implementation of the experimental prototype were covered. First, the synthesis of the chosen NTF was carried out and after that, the basic topologies of operational transconductance amplifiers were presented. The telescopic cascode OTA was chosen because of its low power consumption, moderate voltage gain and high unity gain frequency characteristics. Varying the bias current of this amplifier, the transconductance of the input devices can be controlled and then the f_u and slew rate can be adjusted to the values needed in every mode of operation. This can be done by means of an external regulated current source as discussed here. The use of such a current source offers a degree of freedom , which is important given the flexibility that should be exhibited by the present converter. Scaling of the signal levels of the internal nodes of the architecture was also accomplished. Scaling is

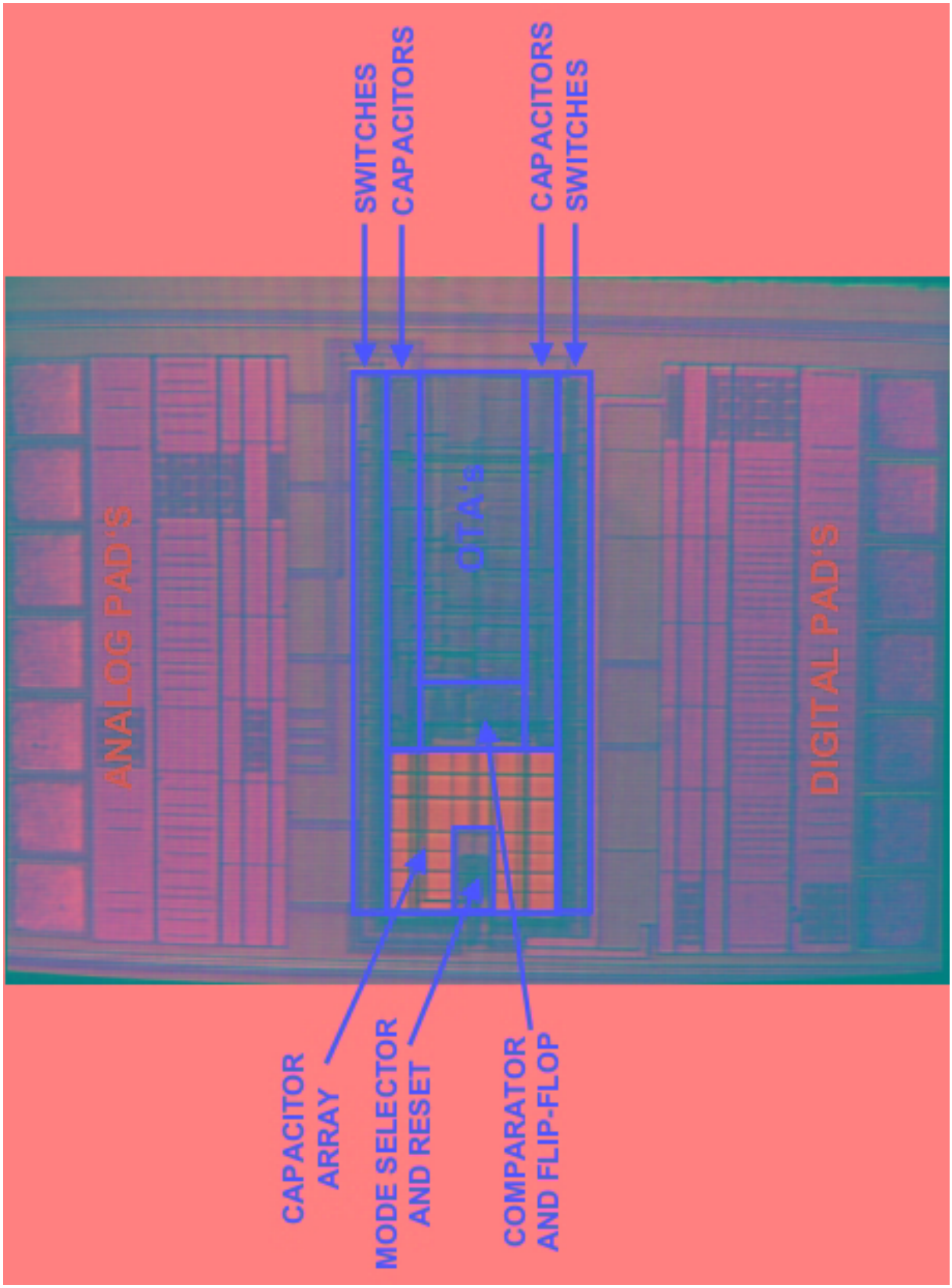

Figure 6.19: Floor plan of the experimental prototype.

a necessary step in the architectural design of any sigma delta modulator in order to have a more uniform distribution of the energy, by reducing or augmenting the signal levels to the desired ones. Here, some of those levels were greatly reduced due to the limited voltage swing exhibited by the chosen amplifier. As observed, two consequences of scaling can be pointed out: first, the capacitive load of the OTA's is augmented by this process. Second, the required voltage gain by the single bit quantizer implementing the comparator is also increased. The first point reveals the necessity of greater biasing currents in the op. amps. in order to reach the *SR* and f_u requirements conducting to a higher power consumption. The second question tells, that aggressive signal scaling in ΣΔM's is not the best way to deal with the reduced dynamic range and poor analog behaviour of the devices characteristic of the technologies owning few hundreds of nanometers and power supply lower as 3 V. The problem of achieving high voltage gain in deep submicrometric or early nano technologies is well known, although the problem envisioned appears at the input of the comparator, lose in charge transfer is also present at the early stages of the modulator, and signal levels with an amplitude of a few millivolts, which result after scaling, can be easily lost due to the charge transfer errors introduced by the op. amp. Non-ideal characteristics.

Behavioral analysis of the proposed modulator was also carried out. Using *MIDAS* the specifications for the OTA's required in the implementation were obtained. With these requirements, four telescopic cascode OTA's were designed together with a regenerative two stages comparator and an output buffer. The global layout of the design was also presented. Care was taken in using separated buses for analog and digital signals, as well as for digital and analog power supply. In the next chapter, the experimental results of the characterization of the present design are going to be addressed.

Chapter 7

Experimental Prototype and Test Results

Contents

7.1 Introduction

An experimental prototype of the proposed 4th order tri mode modulator described in the preceding chapters has been fabricated in a 0.35μm, double-poly, triple-metal CMOS process through EUROPRACTICE. This chapter describes the test setup used to characterize the experimental circuit, and the measured results. The circuit was characterized concerning mainly the achievable resolution and power consumption. As measure of the distortion behaviour only the *SNDR* was taken. Due to restrictions in the characterization equipment, some important proofs as the two-tone test were not carried out; therefore, the intermodulation products were not measured. The chapter begins with the presentation of the printed circuit board designed to verify the unit, following with the obtained spectrum of the output signal of the modulator for the three intended bandwidths. A discussion of the problems encountered during the characterization of the prototype is also introduced. Some suggestions to improve the present design are also given. As a conclusion of the present chapter, the main characteristics of the experimental prototype are presented together with its corresponding figure of merit.

7.2 Test Setup

In order to test the designed circuit a printed circuit board was developed. The die of the fabricated chip was encapsulated in a ceramic J-Leaded chip carrier package with 44 terminals (JLCC 44) and placed in a through hole JLCC socket on the test board. The test board is a two-sided, copper-clad board with separate analog and digital ground planes that are connected together at the power supplies. Analog and digital power supplies were stabilized using surface mounted 10μF tantalum capacitors, that were soldered on the back plane of the board as near as possible to the chip supply pins. An adjustable voltage regulator was constructed using the variable voltage regulator $TL431$ and the low noise rail-to-rail precision op. amp. $LT1677$. This voltage reference was used to generate the needed common mode voltage of 1.65 V. The output of that voltage reference was further stabilized by a surface mounted tantalum capacitor of 10μF.

The biasing currents needed by the op. amps. and the comparator were generated using the adjustable current source $LM134$ and trim-pot's in order to regulate the current to the desired values of 500 and 350 μA, respectively. Silicon area constraints limited the use of more pads, which would have been used to independently polarize every OTA of the modulator. This would have enabled to vary their bias currents in order to adjust the SR and f_u parameters of every amplifier to the values needed in each mode of operation with minimum power consumption. The same constraints forced us to generate inside the chip the biasing voltages required by the transistors constructing the OTA's.

The input test signals were first filtered by means of sixth order bandpass passive LC filters. These filters were designed to drive the 50Ω output impedance of the universal signal generator. The values of the components produce final central frequencies of 107, 240 and 960 kHz. The output of these filters can be selected to feed the RF transformer used to produce the final input differential signal. The RF transformer used here is a one-to-one central tapped device from $Coilcraft$, the $WB2010$. The central derivation of this transformer is fed with the regulated common mode voltage and the outputs are directly coupled to the inputs of the tested chip.

All signals coming from external sources like function or pulse generators were supplied to the board through BNC jacks. Figure 7.1 shows the schematic of the testing printed circuit board.

The required two phases non-overlapping clock signal was generated using the HP 8130A 300 MHz pulse generator, while the input sinusoidal signal was taken from the HP 3245A universal source, which is first filtered and then converted from single-ended to fully differential by the RF transformer on the board.

The complementary digital outputs of the chip were connected to a pair of pin headers and collected in frames of 64k bits by a logic analyzer, which probes have an input capacitance of 18 pF. This signals were connected directly from the chip, since output digital pads with 8mA

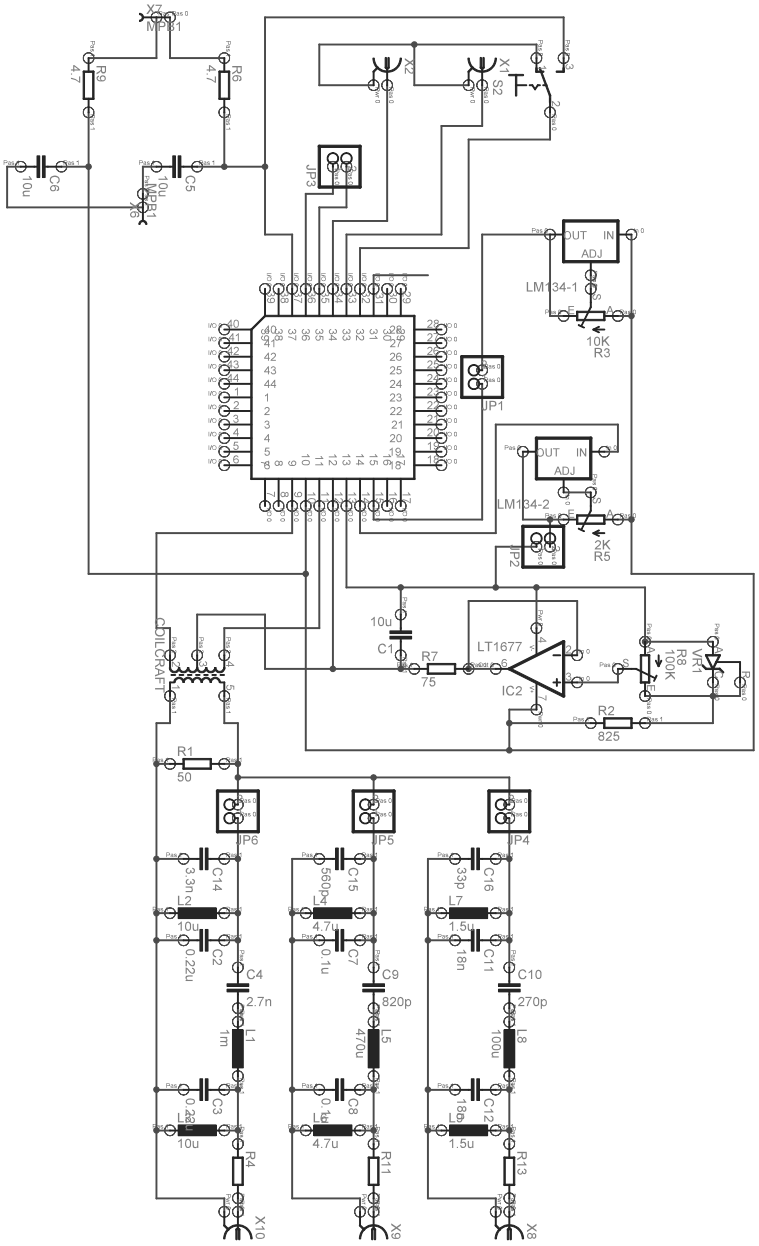

Figure 7.1: Schematic diagram of the PCB used for testing.

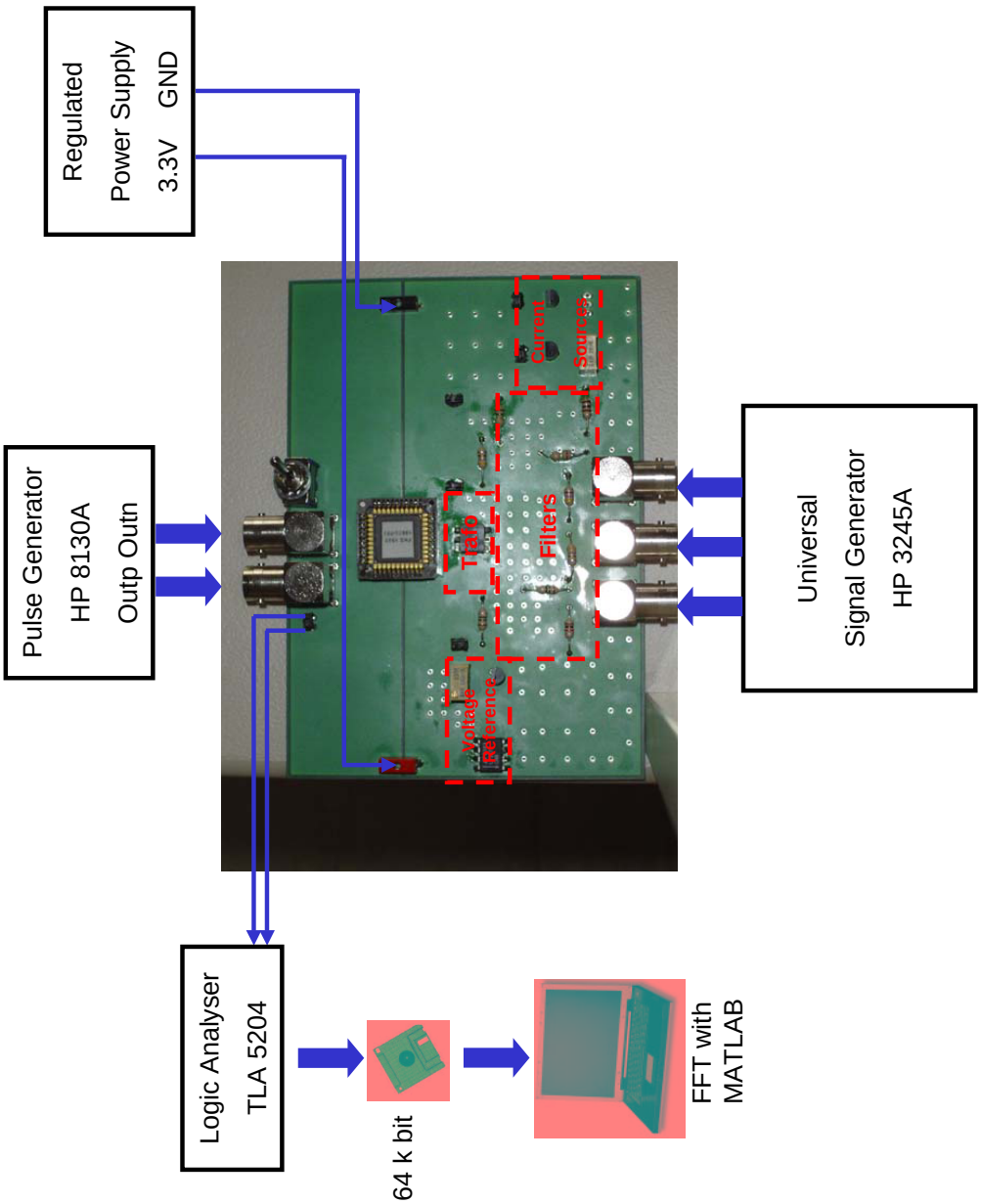

Figure 7.2: Experimental test setup.

strength are being used within the integrated circuit. The complementary 64k bits frames stored in the logic analyzer were further analyzed off-line with *MATLAB*. Figure 7.2 shows a diagram of the experimental setup.

7.3 Test Results

7.3.1 Noise Floor

In order to test the chip performance in the three operation modes, sinusoidal signals with frequencies of 107, 240 and 960 kHz, corresponding to the central frequencies of the passive LC filters, were applied as excitation. The modulator was then clocked with three different frequencies, namely 16, 20 and 76.8 MHz. This corresponds to *OSR*'s of 40 and 20 for the three required bandwidths (200 kHz, 500 kHz and 1.92 MHz). As mentioned, both Q and $\overline{Q}$ outputs were stored and processed off-line with *MATLAB*. For the purpose of canceling the DC offset these frames were subtracted $Q-\overline{Q}$ and then the FFT was computed from the subtracted data, which were first windowed by a Kaiser windowing function with $\beta = 13$. The output signal spectrum can be seen in figures 7.3, 7.4 and 7.5 for each case. The magnitude of the elements of the vector containing the frequency components of the output signal spectrum was normalized to 3.3 before computing the magnitude values in dB. Thus, a zero dB signal has an amplitude of 3.3 V according to this normalization. These three spectra were calculated for input signals with an approximated amplitude of 1.04 V, where the best *SNR* was found.

The capacitors implementing the coefficients g_1 and g_2 were disconnected for the test with the 107 kHz input and connected in the other two cases. The effect of the two resonators can still being appreciated in the last two spectra.

In each spectrum, the noise floor rises as the frequency approaches DC. This is mainly due to the always existing DC coupling coming from the common mode voltage (1.65 V), which is only partially cancelled with the subtraction of Q and $\overline{Q}$, since a mismatch in the differential paths of the modulator exists. Low frequency noise that comes from the power supply is also a cause of these disturbances. The biasing voltages for the OTA's are being produced within the chip using the circuit show in figure 7.5.

In that circuit, the current Ibias was not possible to be generated with the commercial regulated current sources since they need a minimum voltage of 900mV between their terminals for proper operation. Circuit simulations show that the voltage drop introduced by the diode connected P devices is equal to 2.7 V when they are conducting 500 μA as required by the design. This leaves only 600 mV, which are not enough for the appropriated polarization of the current source. For this reason, in that pin only a variable resistor was added for closing the path to ground. Its

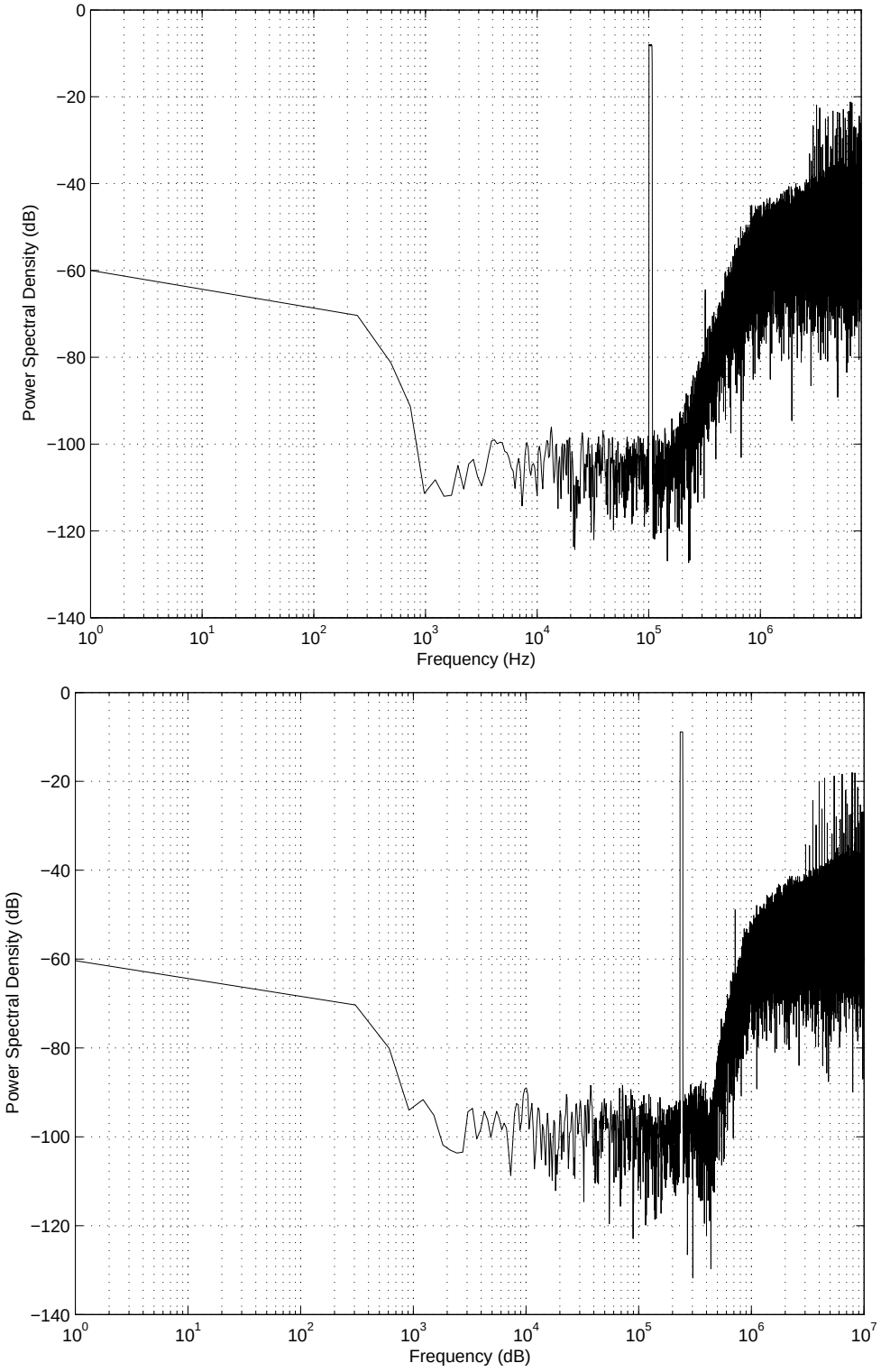

Figure 7.3: Output signal spectrum for the GSM and BT bandwidth.

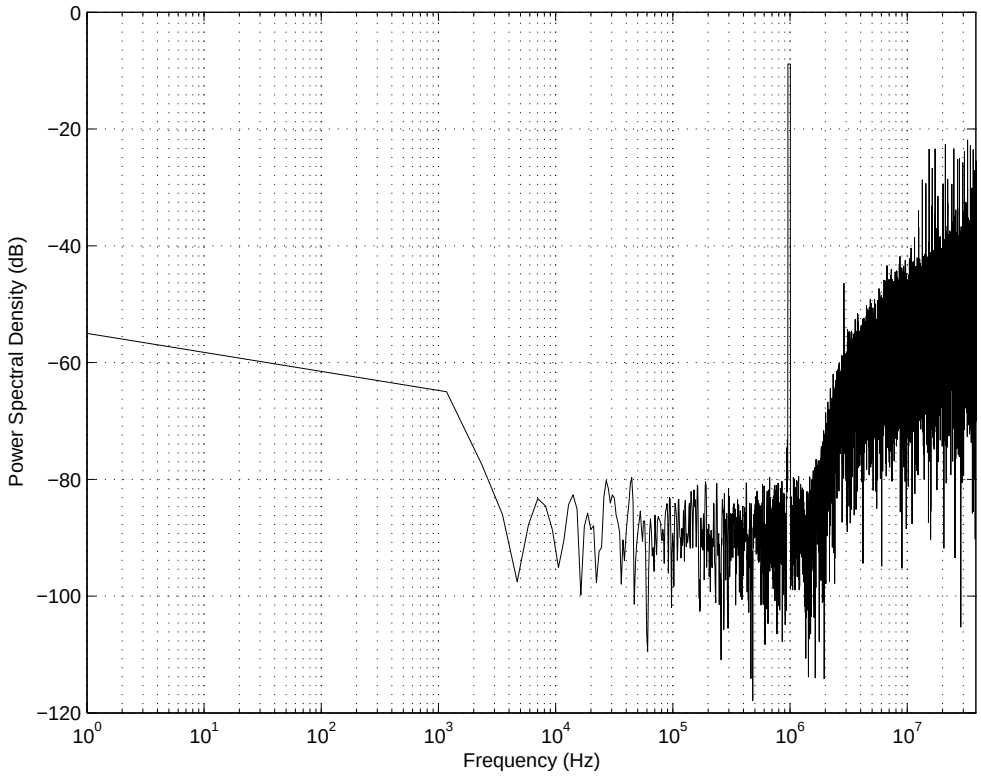

Figure 7.4: Output signal spectrum for the UMTS bandwidth.

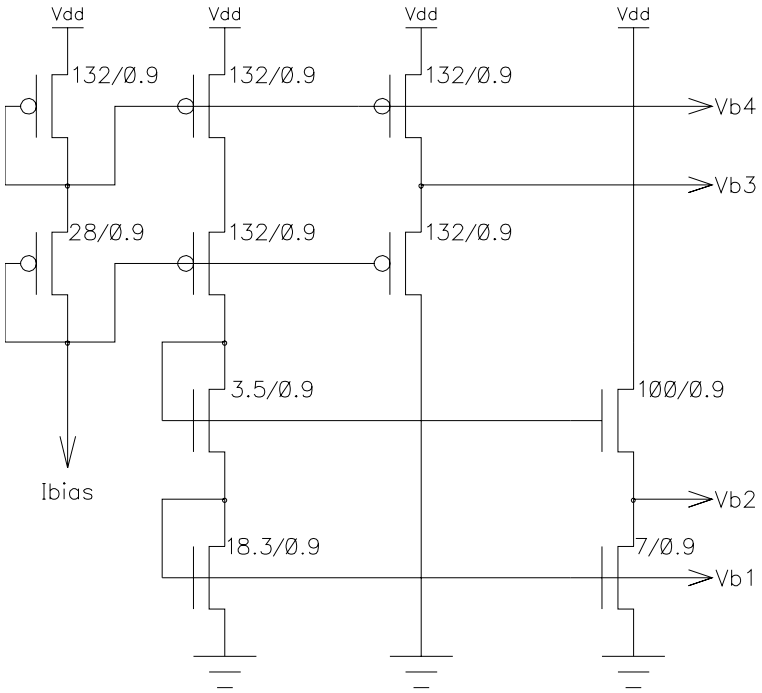

Figure 7.5: Bias circuit.

value was adjusted in order to reach the needed current. This brings as a consequence, the generation of the biasing voltages without any rejection of the power supply. Although the used voltage sources are regulated, any fluctuation in the supply voltage reflects directly into the biasing levels of the transistors in the OTA's. It is well known that fluctuations in a voltage source follow the frequency of the AC line.

The $1/f$ noise of the transistors of the differential pair in the first op. amp. have only a very marginal contribution to this low frequency noise peak. Circuit level noise simulations performed on the input amplifier reveal an input referred noise at DC -111dB under the comparator output levels. Therefore its role is negligible. Other noise contributions that rise the noise floor are coupling mechanisms present in the PCB, impurities in the input signal, as well as quantization noise, thermal noise (kT/C), op. amp. noise and clock jitter. According with eq. 5.11 the quantization noise power should be -100dB and the thermal noise power -118dB, normalized to quantizer output. These values agree approximately with the results obtained by the test done with an input tone at 107 kHz and a clock of 16 MHz. The rising noise floor observed by the test performed with 20 and 76.8 MHz suggest that clock jitter begins to play a more important role. At 76.8 MHz clock frequency, the increment of approximately 10 dB in noise floor must obey a combination of clock jitter together with nonlinear operational amplifier settling. This supposition is reinforced by the observed increment in noise floor as the input signal decreases at the highest sampling frequency. This degradation was not observed in the other two cases. This nonlinear mechanism mixes the input signal with out of band tones at $f_s/2$, since the out of band noise is coloured by the input signal and large tones appear at half of the sampling frequency as the input is decreased.

7.3.2 Resolution and Distortion

Figure 7.6 show plots of the measured *SNR* and *SNDR*. As mentioned before, *SNDR* was the only measure made to characterize the distortion introduced by the designed converter, as a second input signal source was not available. Due to the already mentioned problems with DC couplings, the first four amplitude values of the frequency bin were not taken in order to estimate from the spectrum the mentioned parameters. Otherwise taking the whole of the values would conduct to a very poor resolution performance. This DC coupling problem should be minimized by re-designing the PCB and the used biasing circuit, so that a regulated current source with good PSRR can be used to provide the needed current.

The plots of the *SNR* and *SNDR* versus input signal level shown in Figure 7.6 indicate that the experimental prototype achieves a peak signal-to-noise ratio (SNR) of 72 dB in a frequency band of 200 kHz, 63 dB for 500 kHz and 53 dB for 1.92 MHz.

The traces of both parameters display the increasingly noise floor and degradation of the linear performance for wide band signals, where the sampling frequency used was 76.8 MHz. As it

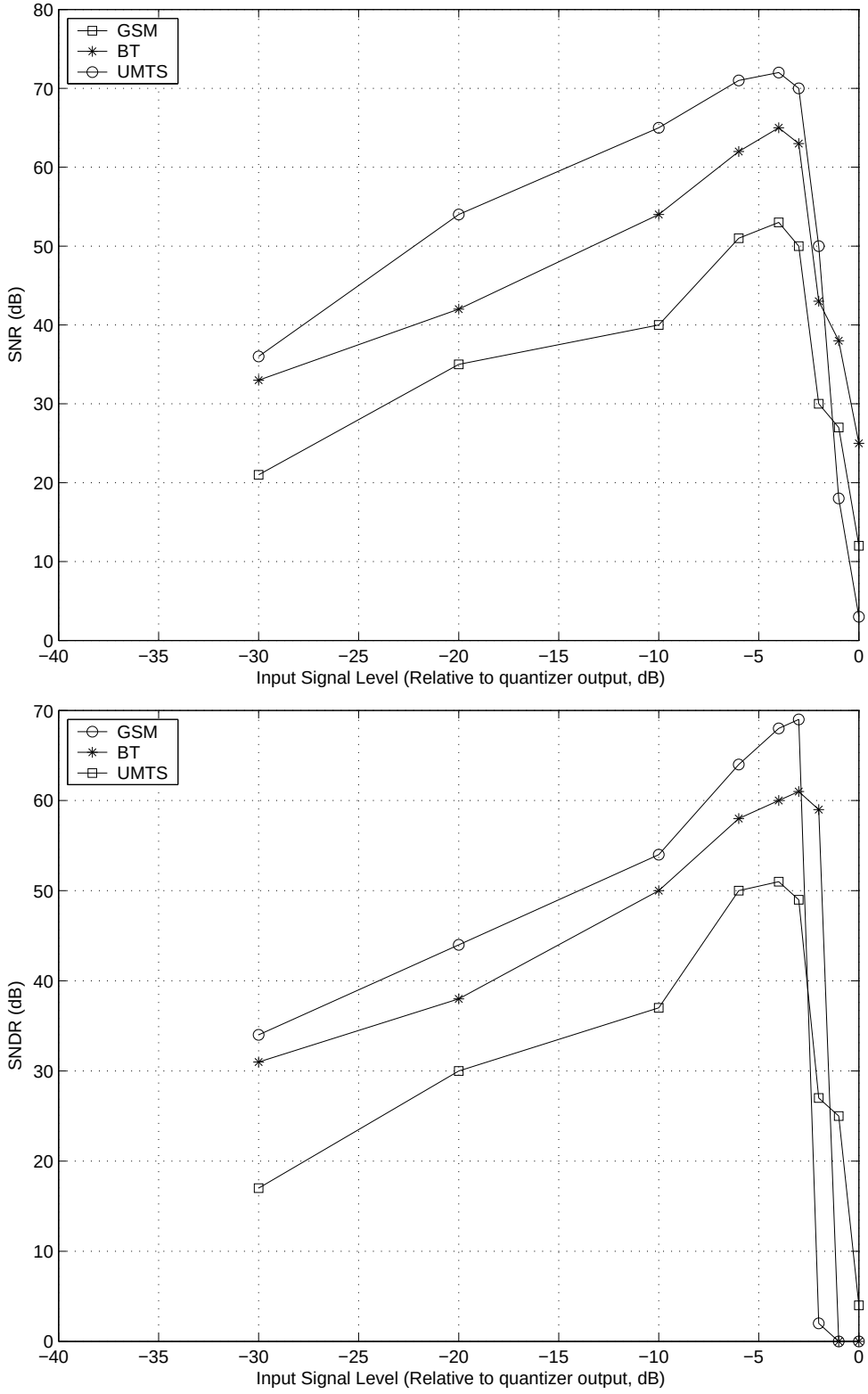

Figure 7.6: Measured *SNR* and *SNDR*.

can be observed from the table 6.5, the input transistors of each OTA are not very wide, this conducts to the somewhat poor values of f_u and non-minimal noise. Keeping in mind the results given in chapter 5 concerning the sensitivity of the taken resonator with respect to OTA finite f_u, where it was seen that even though the deviation of the resonant frequency is not very high, the reduction of the resonant peak is considerably larger. As shown in figure 5.15, an acceptable degradation of the Q factor of the resonant frequency would be obtained by using amplifiers with a f_u of $4f_s$. None of the designed OTA's obey this restriction. The behavioral simulations of the last chapter indicated a minimum f_u of $3f_s$, this discrepancy is due to the model used by the adopted behavioral simulator, which assumes the exponential portion of the response of an OTA within a capacitive feedback as perfectly linear, therefore analysis with this model suggests that a high resolution sigma-delta modulator can be constructed with low bandwidth and high slew rate OTA's. In reality, exponential response is never perfectly linear and high-resolution data conversion is difficult to achieve with low f_u op. amps.

For the other two cases with lower sampling frequency the linearity was well behaved. It should be mentioned that the peak *SQNR* expected for narrow band signals was around 96 dB as the behavioral simulations of chapter 5 showed, where only the effect of quantization noise was taken into account. Then some 24 dB are being lost in the experimental prototype. In the real system, the resolution is being limited by the combination of thermal and op. amp. noise. As mentioned in the last paragraph, the op. amps. should be optimized in order to improve their frequency response and input referred noise by directly augmenting the aspect ratio of the differential pair. Circuit level simulations show that increasing by six the aspect ratio of the input transistors of the first OTA would reduce its input referred noise by 6 dB.

The best performance was obtained by the second case, where the sampling frequency was 20 MHz and the maximum expected *SNR* was 66 dB. Here only 3 dB are being lost, which is a reasonable loss when taking into account all the coupling effects that are present in the final real testing system.

In every curve of figure 7.7, the overload experimented by the modulator is clearly seen if strong signals over -3dB of attenuation with respect to quantization levels are applied at the input. This is a typical behaviour of every sigma delta modulator and does not represent a problem since in practice it is very unusual that such a high input signal is presented in a wireless reception system.

7.3.3 Figure of Merit

In order to compare a particular design with other existent solutions a figure of merit (FoM) should be defined. There are many FoM's proposed in the literature regarding ADC's. For Nyquist rate converters, many authors have adopted the following FoM [62]:

$$FoM = \frac{4kT \cdot DR \cdot f_N}{P} \tag{7.1}$$

Here *DR* states for the converter's dynamic range in absolute value, f_N for the Nyquist sampling rate and *P* for the power consumption. This FoM has been modified in order to take into account the oversampling process inherent to sigma delta converters [63]:

$$FoM = \frac{4kT \cdot DR \cdot BW}{P} \tag{7.2}$$

Where *BW* indicates the bandwidth of interest managed by the converter. The last equation can be modified to take in consideration the linearity performance of the converter if the *DR* is replaced by the *SNDR* in absolute value:

$$FoM = \frac{4kT \cdot SNDR \cdot BW}{P} \tag{7.3}$$

These equations do not include the impact of the technology used in the design as well as power supply, core area and oversampling ratio. These are important parameters for comparison purposes when a design has to be evaluated. In [64] a FoM, which uses five generic parameters was introduced:

$$FoM = \frac{a_1^{ENOB} BW^{a_2} V_{dd}^{a_3} L^{a_4}}{P} \cdot a_5 \tag{7.4}$$

Where *BW* is the input bandwidth, V_{dd} is the supply voltage and *L* the minimum feature size. *ENOB* is the number of effective bits at *BW*. The generic factors $a_{1...5}$ were fitted using data from actual implementation of three types of converters: flash, pipeline and (the analog portion of) Delta Sigma modulators, published in recent years in both the IEEE Journal of Solid State Circuits and the proceedings of the International Solid-State Circuits Conference. For the Delta-Sigma modulator only the low-pass kind was considered. The fitting process was performed using a least mean squares error (LMS) criterion. The reported values of the coefficients for ΣΔM's are given next:

$$a_1 = 1.78$$

Standard	FoM (10^5)
GSM	2.91
BT	2.76
UMTS	2.88

Table 7.1: Estimated FoM

$$a_2 = 0.76$$

$$a_3 = 1.4$$

$$a_4 = 0.18$$

$$a_5 = 0.006$$

The factor a_5 is a scaling factor, which units were chosen such that the total expression is dimensionless. This last FoM was taken in order to evaluate the present design. Numbers for the three different managed bandwidths were obtained and are given in table 7.1. The $ENOB$ was estimated from:

$$ENOB = (SNDR - 1.76)/6.02$$

The power consumption, estimated from measurements and circuit level simulations, indicate a value of 48.57 mW for the analog part of the modulator, including the biasing circuit and the comparator.

Since the solutions for multi-standard A/D converters comprise both LPΣΔ and BPΣΔ modulators, for comparison purposes in the next chapter, equation 7.3 is going to be used, although the already mentioned limitations of that FoM could lead only to a crude evaluation.

7.4 Summary

In this chapter, the experimental results of the designed prototype were presented. The main performance parameters were given and a figure of merit for the evaluation of the present design was introduced. Some problems concerning DC offset appeared during the characterization,

Technology	CMOS 0.35μm
Power Supply	3.3V
Power Consumption	Analog Part: 48.6mW, Digital Part: 8mW
Core Area	0.19sqmm
OSR	40/20/20
f_s	16/20/76.8 (MHz)
BW	200kHz/500kHz/1.92MHz
SFDR	50dB/50dB/45dB
SNDR	69dB/61dB/51dB
SNR	72dB/63dB/53dB

Table 7.2: Performance Summary

this was due to bad-dimensioned P channel devices used in the biasing circuit. The presence of these noises degrade the performance of the device under test and were intentionally left out for the purpose of obtaining the *SNR* and *SNDR* parameters. These problems could be reduced by redesigning the biasing circuit or by adding more terminals to the circuit in order to provide the bias voltages from external regulated voltage sources. The linearity performance of the prototype was not adequate for wide band signals. This is mainly due to the reduced f_u of the OTA's in the design. The transistors present in the differential pair of each op. amp. should be redimensioned as it is the case of the transistors in the biasing circuit. This chapter is closed with table 7.2, where the characteristics of the present design are summarized.

Chapter 8

Conclusions and Future Work

Contents

8.1 Summary of Results and Research Contributions

This thesis was mainly concerned with analysis, modeling and design of ΣΔ modulators, whose characteristics could be adjusted to the requirements imposed by different wireless standards, being so suitable for use in multi-mode cordless receivers.

Based in the experience transmitted by the reported previous approaches, this work proposes to carry out the digitization of signals belonging to narrow band standards at low values of IF. Analog to digital conversion at zero IF is proposed for standards owning a wide bandwidth. As discussed in chapter one, the constant scaling process experimented by the technology has set a barrier in the performance attained by the A/D converters that have been designed in every technology generation. In contrast, the performance depicted by RF front ends has been improved as technology scales. This situation has leaded us to the conclusion, that future receiver architectures will have more efficient and power-full radio frequency sections. This can help to alleviate the not so favorable position envisioned for analog-to-digital interfaces. As the quality that should be displayed by both the ADC and the RF front end embedded in a wireless receiver are close related, higher dynamic range and linearity can be demanded by the radio frequency section of the receivers in order to relax the requirements imposed to the A/D converters that should be designed in future technologies with less than 100 nm.

However, the always-growing bandwidth exhibited by the communications standards, will always ask for higher sampling frequencies. In this work, the use of Single Bit High Order ΣΔ Loops was explored in order to achieve high resolution over wide bands at low oversampling ratios, in order to preserve low power consumption.

Digitization of wideband signals at base band through Single Bit High Order ΣΔ modulators is better accomplished making use of resonators embedded in the filter loop, in order to suppress the quantization noise at different points in the band of interest. In this thesis, two alternatives reported in the literature to construct a resonator using the switched capacitor technique, were analyzed and compared. Such an analysis and comparison was not found in the literature for resonators at f_s/n with $n > 4$ at the time of writing this thesis.

It was found, that the biquad section constructed with integrators has better characteristics concerning the robustness against the main circuit non idealities present in a switched capacitor realization when compared to the behavior of second order sections synthesized with delay elements. This study was restricted to the effect introduced by finite voltage gain (A_V), non zero input capacitance (C_{in}) and finite unity gain frequency (f_u) that characterize the operational transconductance amplifiers (OTA's) used in the implementation of those resonators. The effect of capacitor mismatch was also reviewed by means of Monte Carlo simulations.

The flexibility offered by Single Bit High Order ΣΔ modulators was also subject to investigation in this work. Ideally an architecture of a high order ΣΔ modulator, should be able to synthesize different types of noise transfer functions by simply changing its coefficient set. In practice, the realizable functions will be limited by the characteristics of the operational amplifiers used in the realization of the architecture under question. In this approach, the set of coefficients of a fourth order architecture, was changed to produce two different noise transfer functions: a Butterworth-like noise transfer function with all zeros at DC using a cascade of integrators with feed forward coefficients for high resolution A/D conversion of narrow band signals and the same NTF plus two transmission zeros using a cascade of resonators with feed forward coefficients for low resolution wide band signals.

The superior performance exhibited by the integrator based resonator when producing resonant peaks at f_s/n encouraged its employment by designing an experimental prototype used to proof these ideas.

Given the results of the analysis of the resonant structures, it was desired to show with the design of the experimental prototype, the feasibility of achieving enough resolution/speed performance using standard circuit techniques such as single stage amplifiers and transmission gates as switches.

The experimental prototype was fabricated in a 0.35μm double-poly triple-metal N-well CMOS technology. This design occupies an area of $1mm^2$ including bonding pads. Test and characterization of the proposed converter were also carried out. In order to evaluate the presented

solution and to have a comparison with other solutions for multi-standard reception, the FoM's given in equations 7.3 and 7.4 were applied to the numbers obtained in this work as well as those given in [3] and [4]. The results of this comparison are given in figures 8.1 and 8.2.

The work presented in [39] was included in the comparison presented in figures 8.1 and 8.2 for the case of wideband signals, in that work, a continuous time fourth order prototype using a 1.5 bit quantizer aimed for digitization of UMTS signals at base band was presented. The results presented in figures 8.1 and 8.2 could help us to reinforce the adopted premise of digitization of wide band signals: It can be efficiently accomplished at base band rather than at high values of IF.

The designed prototype is aimed to be used as an A/D interface of a multi-mode receiver architecture developed in another work concerned with modelling and design of RF front ends. That receiver architecture was designed trying to follow the tendencies given by the behavior of the analog and RF systems as technology scales and presented in chapter one.

8.2 Recommended Future Work

After a work has been done, another must be started. The research developed here suggests tasks in two directions: Improvement of the proposed solution and to seek for alternatives to overcome the aspects of this approach, in which some weaknesses have already been envisioned. For the purpose of improving the designed sigma delta modulator of this thesis the following efforts should be accomplished:

Reduction of the kT/C noise

The noise being sampled and therefore aliased at the input of the modulator can be reduced by augmenting the input-sampling capacitor. In the present design, this can be directly done without further increasing in power consumption by changing the position of the resonators. From table 6.2 and figure 6.11, if the position of the resonators were interchanged, the input capacitor would be equal to 350 fF, this would bring a reduction of more than 50 per cent in the kT/C noise value. The third operational amplifier has also a higher *SR*, this in turn would help also to improve the linearity of the whole converter, since the errors introduced by this op. amp. would be lower, the errors introduced by the other OTA's are subject to noise shaping and for that reason they introduce a weaker effect.

Reduction of the clock jitter effect

Due to the low *OSR* being used, the effect of clock jitter in the performance of the designed prototype has been seen. The rising noise floor observed for clock frequencies equal to 20 and

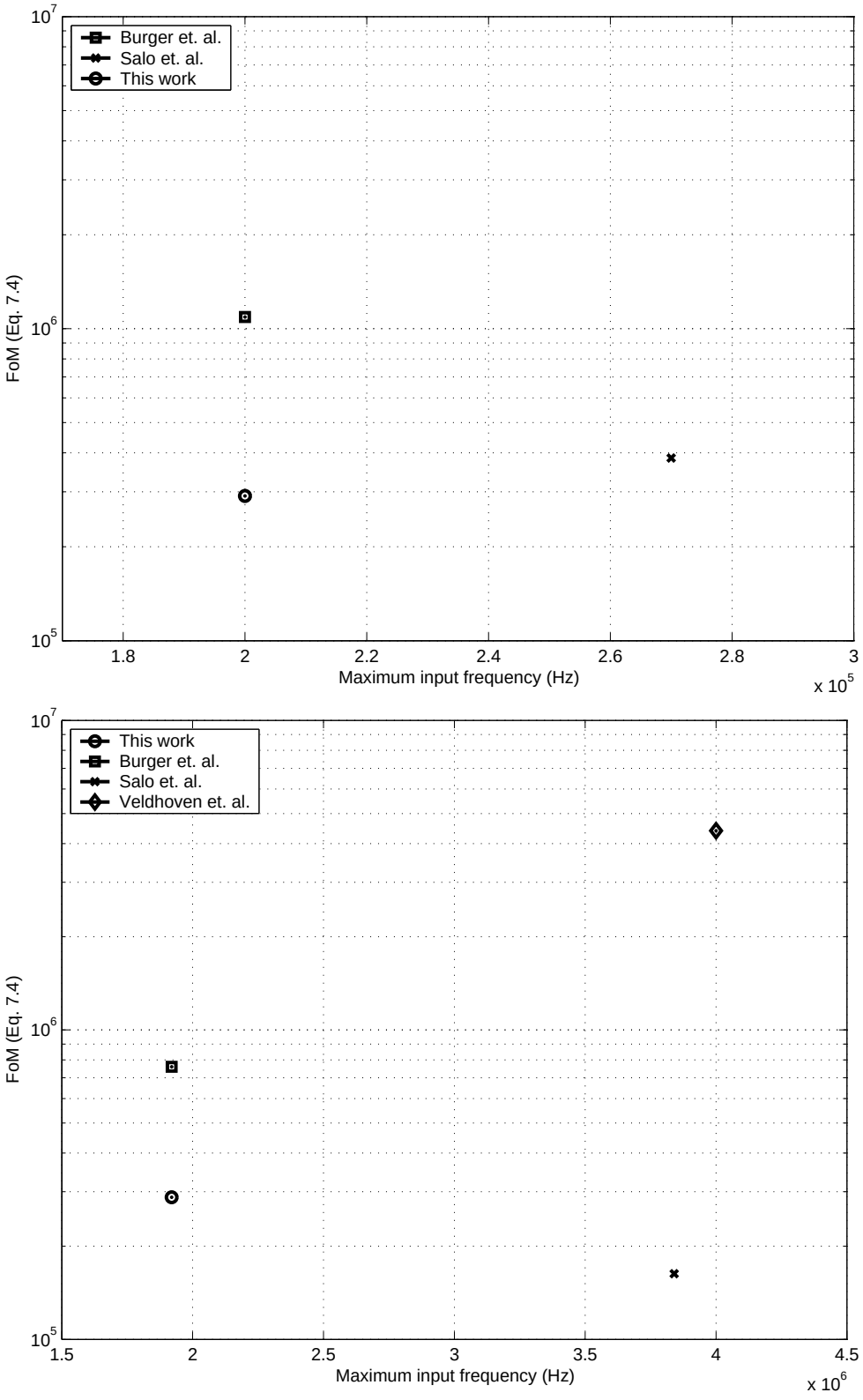

Figure 8.1: FoM after eq. 7.4.for GSM and UMTS signals

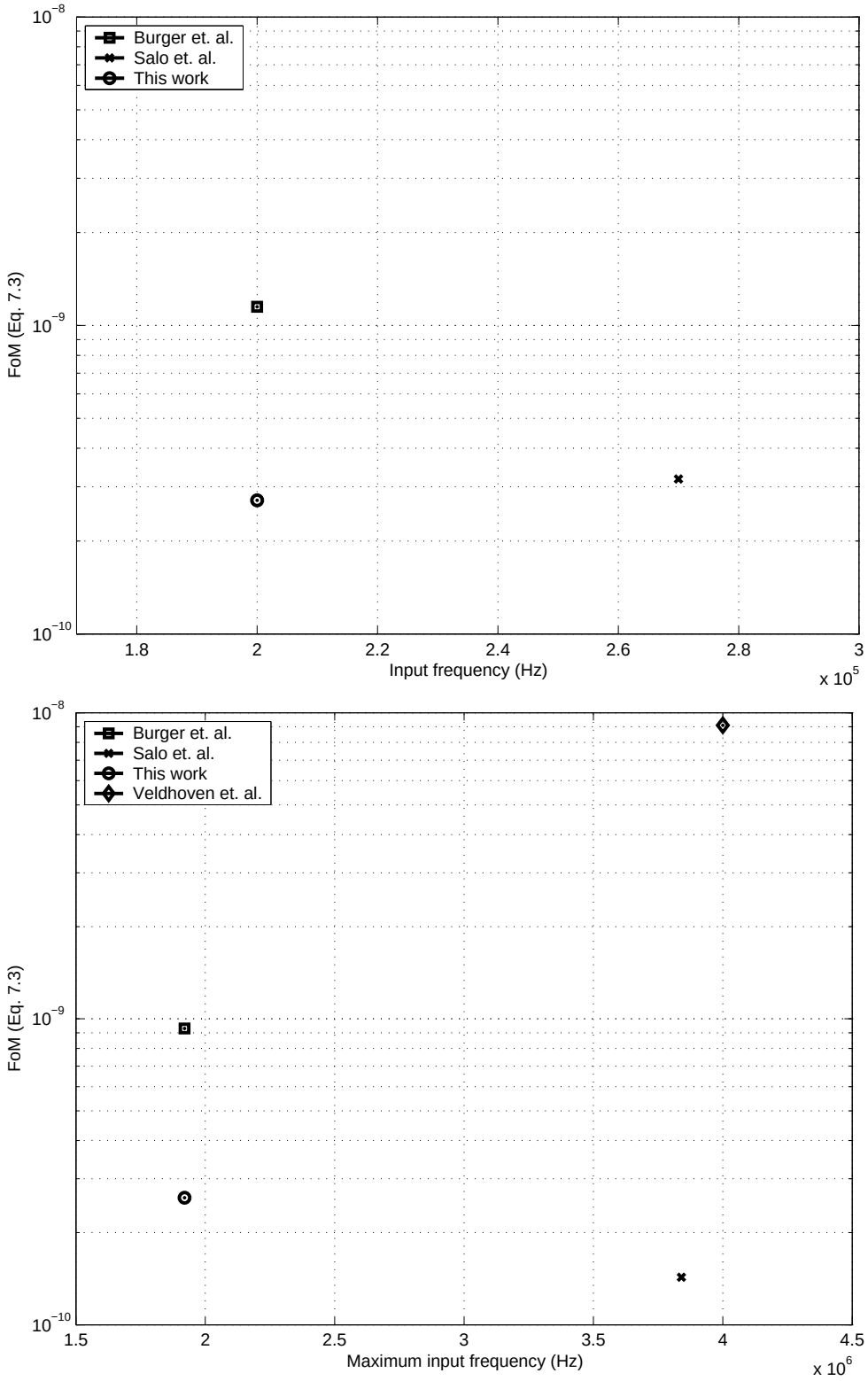

Figure 8.2: FoM after eq. 7.3.for GSM and UMTS signals

76.8 MHz indicate, that clock jitter play a more important role in the system. This effect can be reduced if the quality of the switches being used in the experimental prototype is improved. Investigations in this topic have found, that the use of Bootstrapped switches represents a good alternative in order to minimize the effect of clock jitter. Although this would represent a considerable effort in layout, the gain in performance for wide band signals can be seen as a good motivation to accomplish this task.

Improvement of the PSRR

As mentioned in the previous chapter, the designed biasing circuit does not permit to use regulated current source to provide the necessary biasing current. This brought as a consequence a poor *PSRR* in that circuit, which bring slow changes in the polarization voltages of each OTA. The effect of this problem was reflected as DC offsets and higher noise at low frequencies, which degrade the *SNR* of the prototype. The transistors comprised by this circuit must be resized in order to allow the presence of an external regulated current source with good *PSRR*, which should help to reduce the low frequency noise present in the spectrum of the output signal coming from the experimental prototype. Another way to overcome this situation is to allow for the use of more bonding Pad's and to provide the needed polarization voltages from external regulated voltage sources.

Design of a finite state machine

In order to guarantee the stability of the present design a finite state machine, which counts the one's at the output of the modulator should be designed. This machine should provide the necessary reset to the integrating capacitors of each stage of the modulator, if a long chain of one's or zero's is taking place. This would be a sign, that instability through overload of the output of the integrators is starting to happen. This would be avoided by completely discharging those capacitors through switches controlled by the mentioned digital machine.

Review of the linearity

The linearity of the proposed solution should be verified experimentally. As mentioned in the last chapter, the two-tone test was not carried out due to limitations in the testing equipment. In order to have number representing the linearity of the device under test the two tone test should be carried out injecting at the input both test signals in band and a large interferer out of band. This test would give a better estimation of the linearity of the present design as well as of its spurious free dynamic range performance.

There are mainly two aspects in which the proposed solution shows problems that limit its application in future technological scenarios with further reduced power supply voltages or wider band signals, which would ask for higher sampling rates. These questions are listed bellow:

Internal signal swing scaling

As observed in chapter 6, the internal signal swing scaling process required to keep the signal levels within the linear operation region of the operational amplifiers, inherently augments the capacitive load seen by each OTA. This in turn increases the power consumption after a *SR* and f_u requirement has been given. In this sense, single stages of amplification such as the folded cascode OTA or the telescopic OTA lose their attractiveness concerning the trade off speed/power consumption. A more relaxed signal swing scaling should be needed if a two-stages OTA would be used. Here, the reduction in capacitive load together with the, in principle, higher power consumption of a two-stages OTA should be evaluated in order to find out the proper solution; of course, as power supply voltage goes down to levels of 2.5V or lower, the use of the Miller-compensated two-stages OTA is mandatory.

Having in mind the emerging CMOS technologies as well as the wider frequency bands to be converted, a valuable investigation would be to explore low voltage techniques, such as *the switched op. amp. technique* for the digitization of wide band signals, since those techniques have been until now proposed only for the case of narrow band signals like voice [65, 66, 67] or GSM [68]. For middle bandwidth signals like BT, this technique was appied in [69], where very low *SNR* was required.

Unity gain frequency requirements

As seen during the development of the presented design, the required f_u, that an operational amplifier must posses, in order to construct a good integrator based resonator, lays on the order of $4f_s$ this requirement translates to fairly high speed requirements as the bandwidth to be converted augments. In the present design, the used size of the input transistors of each OTA allow to improve this characteristic in every element, however, in some of them it would be very difficult to reach the required value due to the large capacitive load, as is the case of the first OTA used in the design. This problem suggests the use of improved versions of the operational amplifiers, namely, the employment of the gain enhancement technique. It is known that the use of gain boosting techniques in the op. amps. also improves the frequency response of them. In this way higher values of f_u can be reached. However the optimized design of gain-boosted OTA's is not an easy task, that asks for computer optimization techniques.

In order to attack this problem, the use of N-Path techniques to design a high quality resonator at f_s/n with $n > 4$ should be reviewed. It is well known that such resonators within bandpass sigma delta modulators have helped to reduce the needed f_u of the OTA's present in the implementation of those modulators. These techniques should be translated to the lowpass case of sigma delta modulators aimed for the digitization of wide band signals at low oversampling ratios. This is important for future applications of sigma delta converters in communications systems, where the added services of those systems are going to ask for wider frequency spectra.

Appendix A

Estimation of the in-band quantization noise power using Taylor series

Here, the approach used in chapter 3 as well as in [33] to estimate the in-band quantization noise power is presented. Equation 3.13 was solved by using the approximation $\sin(x) \approx x$. It is possible to use this simplification mainly because of the following two reasons: the BW is a very small fraction of f_s, this means $f_b << f_s$ and secondly: we are interested in knowing the behaviour of the noise only in a small region within the normalized frequency axis, since the out of band noise is assumed to be rejected by an ideal digital filter.

The mentioned approximation, enable us to solve the integrals required to estimate the quantization noise power within the band of interest for lowpass modulators having a pure differencing NTF as well as for bandpass modulators whose resonators have been derived by means of the transformation $z^{-1} \rightarrow -z^{-2}$, since the resulting NTF has usually the form $(1+z^{-2})^n$.

However, stabilized single bit high order $\Sigma\Delta$ loops posses NTFs that do not correspond any more to the family of functions already mentioned. For BP$\Sigma\Delta$Ms, whose resonators were not derived by the cannonical transformation and for stabilized single bit high order $\Sigma\Delta$Ms the resulting NTF is rather a rational function of z with order n in which, the evaluation of the bounded integrals by hand using the susbstitution $\sin(x) \approx x$ could become very difficult.

In such cases, the use of programms for symbolic computation is a powerfull tool, which significantly simplifies the work. There are many programms available at the market, each of them with different characterisitics and more or less friendly user interfaces. Due to its importance, almost any of them includes the *Taylor series expansion* of one-dimmensional functions around a point.

The one-dimensional Taylor series expansion of a real function $f(x)$ about a point $x = a$ is given by:

$$f(x) = f(a) + f'(a)(x-a) + \frac{f''(a)}{2!}(x-a)^2 + \frac{f'''(a)}{3!}(x-a)^3 + \ldots + \frac{f^{(n)}(a)}{n!}(x-a)^n \quad \text{(A.1)}$$

Observing the last equation and due to the reasons mentioned in the first paragraph, it is possible to expand, using Taylor series, the rational function of z representing the NTF of the modulator under analysis around the normalized frequency of interest. Using a symbolic processor, this is only a matter or writing some code lines. After that, by taking the first term of the series, we have an estimation of the value of the module of the NTF under question. This term can be used to substitute the whole function and to evaluate the integral within the BW of interest.

We used the symbolic processor *MUPAD* from which, an evaluation version can be downloaded form $http://research.mupad.de/$. In this programm, comments are added to the code by preceeding it with a double slash (//). Next, the codes needed to analyse the architectures of the BPΣΔMs presented in figures 3.19 and 3.22 are given. The reader can run these codes in order to find: in-band quantization noise power (Pq), signal-to-noise ratio (SNR) and dynamic range (DR) for both architectures.

```
//Analysis of figure 3.19:
//Signal transfer function:
A:=1/(1+z^(-2));
B:=-z^(-2)/(1+z^(-2));

N1:=x-y;
N2:=N1*A;
N3:=N2-y;
N4:=N3*B;
STF:=solve( y=N4 , y );

//Noise transfer function:
t:=-y;
u:=A*t;
v:=u+t;
w:=B*v;
NTF:=solve(y=w+n, y);

//In-band quantization noise power:
Nq:=op(op(NTF),2);
Nq:=simplify(Nq/n);
NQ:=subs(Nq , z=exp(2*PI*I*f));
NQc:=subs(Nq , z=exp(-2*PI*I*f));
NQm:=NQ*NQc;
```

```
NQm:=simplify(NQm);
series(NQm, f=1/4, 5);
Sq:=int((2*256*PI^4*f^4), f=(-Af)..(Af));
Sq:=subs(Sq , Af=f/Fs);
Sq:=subs(Sq , f=Bw/2);
Sq:=subs(Sq, Bw=(Fs/(2*M)));
Pq:=Sq*(d^2)/12;

//SNR:
SNR:=((AMP^2)/2)/Pq;

//DR:
DR:=subs(SNR , AMP=d/2);

//Analysis of figure 3.22:
//Signal transfer function:
K:= 1/2;
A:=((-1/2)*z^(-1))-(z^(-2)/(1+z^(-2)));
N1:=x-y;
N2:=K*N1;
N3:=(N2*A);
N4:=N3-y;
N5:=(N4*A);
STF:=solve(y=N5, y);

//Noise transfer function:
s:=-y;
t:=K*s;
u:=(t*A);
v:=u+s;
w:=(v*A);
NTF:=op(solve(y=w+e, y));

//In-band quantization noise power:
Nq:=simplify(NTF/e);
NQ:=subs(Nq , z=exp(2*PI*I*f));
NQc:=subs(Nq , z=exp(-2*PI*I*f));
NQm:=NQ*NQc;
NQm:=simplify(NQm);
series(NQm, f=1/4, 5);
Sq:=int((2*1024*PI^4*f^4), f=(-Af)..(Af));
Sq:=subs(Sq , Af=f/Fs);
Sq:=subs(Sq , f=Bw/2);
```

```
Sq:=subs(Sq, Bw=(Fs/(2*M)));
Pq:=Sq*(d^2)/12;

//SNR:
SNR:=((AMP^2)/2)/Pq;

//DR:
DR:=subs(SNR , AMP=d/2);
```

Appendix B

Errors introduced by finite OTA A_V in a SC integrator

This appendix shows the derivation of the equation 5.23. A SC integrator whose OTA has finite A_V and non-zero C_{in} is depicted in figure B.1.

Due to finite A_V and $C_{in} \neq 0$ a voltage different from zero appears at the node **n** of figure B1. Under this conditions, the electric charge stored by the capacitances in the circuit when $f1! = 1$ at the instant $(nT-1)$ is equal to:

$$Q_1(nT-1) = -C1 \times V_{in}(nT-1) \tag{B.1}$$

$$Q_2(nT-1) = C2 \times (V_{out}(nT-1) - V_n(nT-1)) \tag{B.2}$$

$$Q_{in}(nT-1) = Cin \times (V_n(nT-1)) \tag{B.3}$$

Note that $V_{out}(nT-1)$ is equal to the voltage at the bottom plate of C2. At the instant $(nT-1/2)$ the OTA and the capacitors are connected as shown in figure B.2

For this circuit the charge stored in the capacitors becomes:

$$Q_1(nT-1/2) = C1 \times (V_n(nT-1/2)) \tag{B.4}$$

$$Q_2(nT-1/2) = C2 \times (V_{out}(nT-1/2) - V_n(nT-1/2)) \tag{B.5}$$

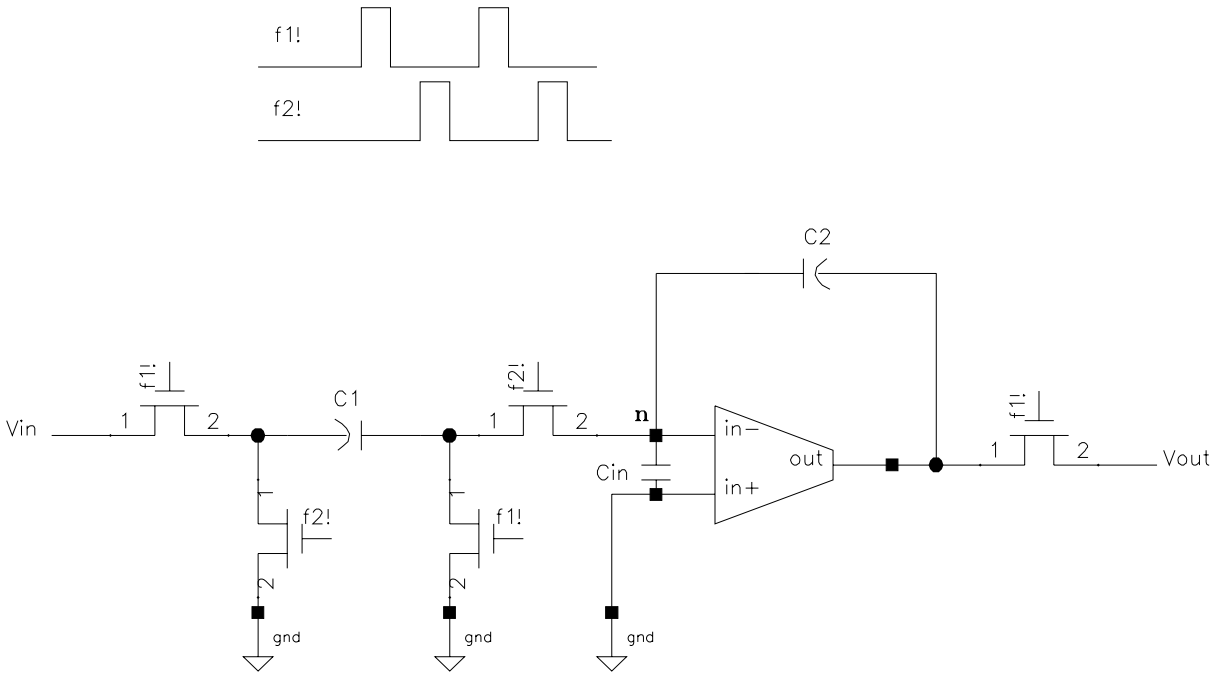

Figure B.1: An OTA with finite A_V and $C_{in} \neq 0$ in a SC integrator

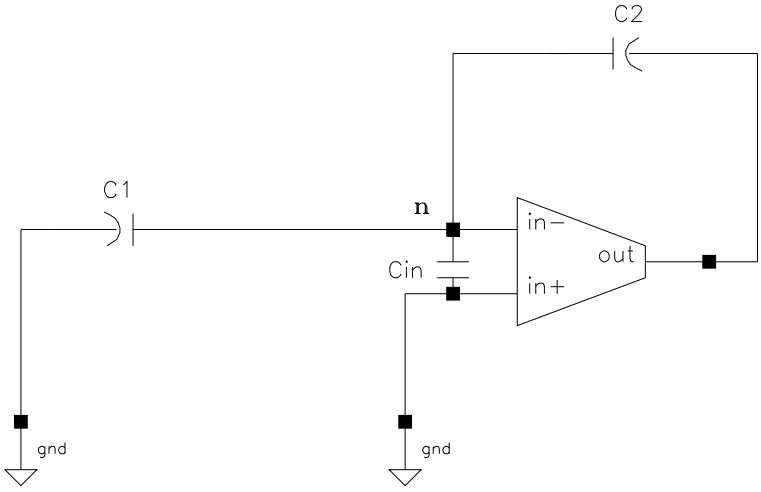

Figure B.2: An OTA with finite A_V and $C_{in} \neq 0$ during charge transfer.

$$Q_{in}(nT-1/2) = Cin \times (V_n(nT-1/2)) \tag{B.6}$$

Electric charge conservation leads to the following expression for the final charge in C2:

$$Q_2(nT-1/2) - Q_2(nT-1) - Q_1(nT-1/2) + Q_1(nT-1) = Q_{in}(nT-1/2) \tag{B.7}$$

At nT the charge in C2 remains and V_{out} equals to the voltage at the bottom plate of C2, thus:

$$\begin{aligned} C2 \times (V_{out}(nT) - V_n(nT)) - C2 \times (V_{out}(nT-1) - V_n(nT-1)) \\ -C1 \times (V_n(nT) + V_{in}(nT-1)) = Cin \times (V_n(nT)) \end{aligned} \tag{B.8}$$

Since $V_n = -V_{out}/A_V$ the solution for $V_{out}(nT)/V_{in}(nT)$ of the last equation produces:

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{A_V C1 z^{-1}}{C1 + C2 + A_V C2 - C2 z^{-1} + Cin - C2 A_V z^{-1}} \tag{B.9}$$

Since the β factor is deifned as $\frac{C_2}{C_1+C_2+Cin}$ the last equation can be re-written as:

$$H(z)_m = \frac{C_1}{C_2} \frac{\varepsilon_n z^{-1}}{1 - \varepsilon_d z^{-1}} \tag{B.10}$$

where:

$$\varepsilon_n = \frac{A_V \beta}{1 + A_V \beta}$$

$$\varepsilon_d = \frac{\beta(1 + A_V)}{1 + A_V \beta}$$

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Supervised Theses

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